Broadband Codecs for an Experimental 224 Mb/s PCM Terminal

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(Manuscript received August 5, 1965)

High-speed PCM codecs (coders and decoders) have been constructed to handle broadband signals such as a mastergroup of telephone channels or an NTSC color TV signal. Two widely different approaches to the realization of the coding function are described. The first and earliest version utilizes a beam coding tube to convert the analog signal to digital form. The second approach employs a tandem array of solid-state stages to perform the required conversion. Associated circuits to implement the filtering, sampling, holding, timing, translation, framing, and decoding functions in a PCM codec are also described. Analysis results, experience gained in design, and measured performance of the coders and the associated circuits that make up a PCM codec demonstrate that they can be produced to meet stringent performance objectives.

I. INTRODUCTION

The design of the coding and decoding complexes of the PCM terminals discussed by Mayo[1] will be covered herein. The term "codec" will be used to denote the coder (analog to digital converter), the decoder (digital to analog converter), and all of the associated circuits, such as sample and hold, parallel to serial converted, Gray to binary translator, resampler, and framing and timing circuits. This definition specifically excludes the multiplexing and demultiplexing portions of the terminal covered in the paper by Witt.[2]

Before the detailed circuit designs are examined, it will be profitable to delineate the two approaches taken to the realization of the encoder. In both coder approaches ideal uniform quantization was sought. The additional quantizing noise advantage attendant to nonuniform quantization was left for future development.

When this project was undertaken only the beam coding tube[3] appeared to satisfy the need for high performance mastergroup and TV

encoding.[4] Even then it was recognized that this was by no means an easy task. A much improved coding tube was required[5] and high-speed, high-accuracy, solid-state circuitry had to be designed to couple the tube to the outside world.

At the same time, several other general approaches to coding were examined to determine an approach that could be realized exclusively with solid-state devices. This study phase led to a proposal for utilizing a novel circuit realization[6] of the folding coder.[7] Considerable uncertainty remained since implementation of the scheme called for the use of solid-state devices on the very fringe of the state of the art.

As expected from the outset, the coder using the beam coding tube achieved the desired performance first. Realization of the solid-state coder proceeded more slowly as each new obstacle was recognized and overcome. To date, the tube coder has outperformed its solid-state counterpart in both speed and accuracy; though this gap is being narrowed. Indeed, improved devices, circuit techniques, and equipment layouts (beyond those described in this paper) are coming into being to support the conclusion that this gap is destined to disappear. There is little doubt *today* that the solid-state coder can be made more economically than the tube coder, and be realized in a considerably smaller package, and can be made more compatible from the equipment standpoint with the rest of the terminal. Though it is clear that the future lies with the all solid-state system, the beam coding tube has served as a very useful stepping stone. Its mere existence was an essential vehicle for exercising other terminal circuits as they came into being. More important, the early realization of the tube coder was used in a field experiment to verify the predicted high quality performance obtainable with a PCM terminal transmitting live mastergroups.[8,9] This was an integral and valuable link in the over-all development program.

Section II covers the beam coding tube and its associated deflection and readout circuitry. Section III is devoted to the solid-state coder design, realization, and performance. Section IV is compartmentalized into subsections describing the remaining circuits that complete the coder. In Section V the circuits in the decoder are described. A brief section on general equipment principles concludes the paper.

II. BEAM TUBE CODER

2.1 *General*

Coding tubes of the ribbon-beam type are particularly well suited to analog to digital conversion where precision and relatively fast coding

times (in the order of several tens of nanoseconds) are required. Tube coders fall into the class of word-at-a-time coders which are inherently fast. All possible code words are stored on the code plate, the code word that corresponds to the analog input is selected by deflecting the beam, and binary decisions on all digits are made simultaneously and independently.

The accuracy of the coding operation is primarily a function of mechanical tolerances within the tube. Considerable progress was made in this area by the Tube Development Laboratory of Bell Telephone Laboratories culminating in the design of the nine-digit Gray code coding tube used in the system.[5]

The tube coder has been operated at a sampling rate of about 12 Mc/s for coding of standard black and white as well as color television signals and at approximately a 6-Mc/s sampling rate for coding of 600-channel single-sideband frequency multiplexed mastergroup signals.

The system block diagram of the tube coder is shown in Fig. 1. The signal is sampled and held and applied to the deflection amplifier which delivers a balanced signal to the two deflection plates of the tube. During the latter part of the hold period the beam is turned on by the grid driver. During this time the parallel PCM output is amplified by linear sense amplifiers and directed to the parallel to serial converter. The serial PCM signal is finally regenerated by the output regenerator.

In the following sections the design considerations of these blocks are discussed in greater detail.

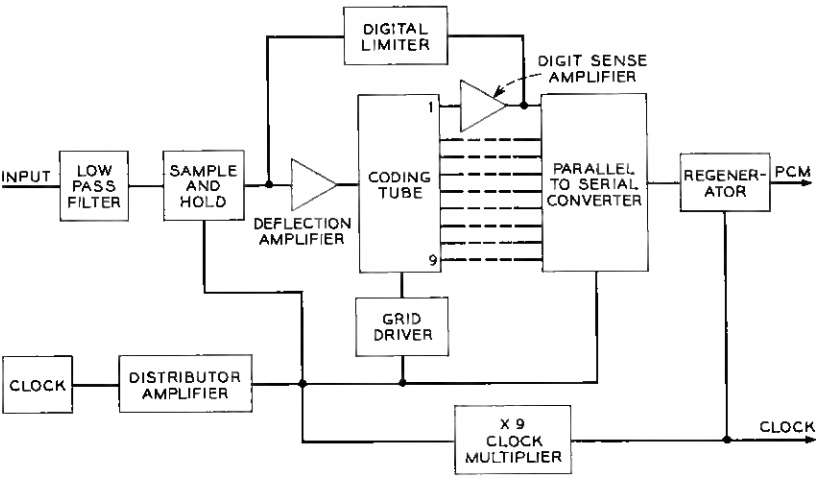

Fig. 1 — Block diagram of tube coder.

2.2 *Coding Tube Description*

As illustrated in Fig. 2(a), a triode electron gun generates a ribbon-shaped beam about one-half inch wide. An electrostatic objective lens system focuses the beam to an average thickness of 2 mils. By means of a pair of tilt electrodes the horizontal orientation of the beam can be controlled by application of an external correction voltage. The analog sample is applied to a pair of vertical deflection plates to direct the beam to the corresponding code position on the code plate. The code plate is perforated with nine vertical columns of apertures (Fig. 2b). The pattern of apertures in each column represents a digit position in a nine-digit Gray code. That portion of the beam which intersects the code plate at an aperture position in a particular column penetrates to the target block and generates secondary electrons. These electrons are

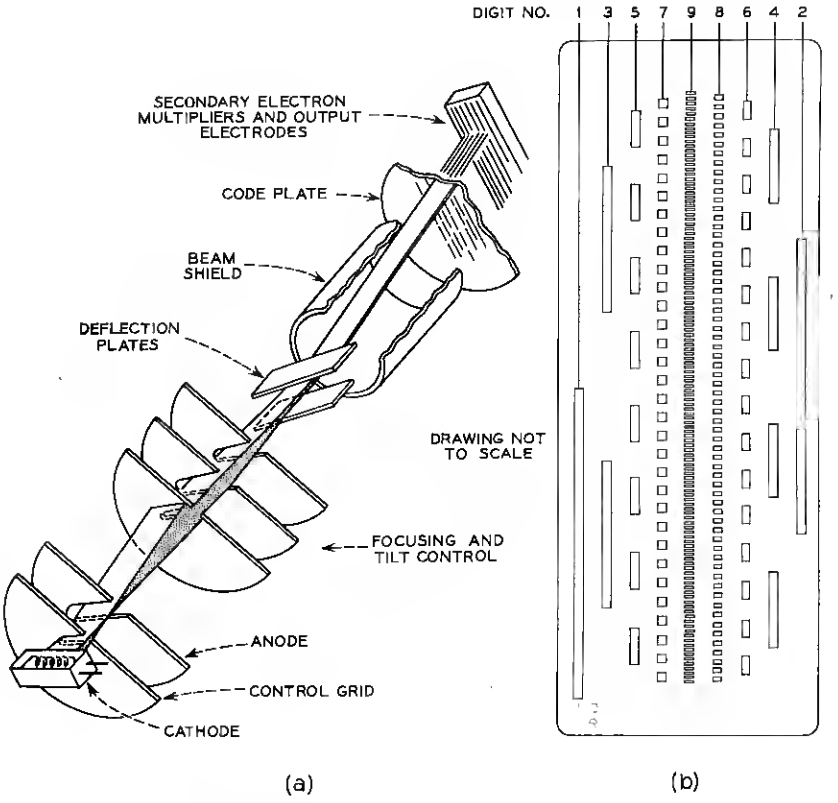

Fig. 2 — Schematic representation of (a) coding tube, (b) 9-digit code plate.

collected by the vertical collector wire assigned to each column. Current flows into an external load and represents a binary ONE in that digit.

A more extensive description of the mechanical details and assembly techniques is given elsewhere.[5]

2.3 *Critical Parameters and Impairments*

2.3.1 *Deflection System*

The two deflection plates form a balanced electrostatic deflection system. Drive voltages of equal magnitudes and opposite polarities are applied to the plates. A peak-to-peak magnitude of 30 volts is required at each plate in order to deflect the beam over the entire code plate. The equivalent capacitance of each plate (measured from plate to ground) is 15 pF.

To avoid coding errors due to external stray electric fields, the beam is shielded in the area between the deflection system and the code plate by a concentric shield. The entire tube is externally encased by a Mu-metal envelope to eliminate interference from stray external magnetic fields.

2.3.2 *Electron Beam*

The accuracy of the coding process is adversely affected by imperfections in the electron beam. Beam thickness, uniformity of current density distribution across the width of the beam, shape, and horizontal orientation are critical characteristics to be considered. Impairments in these parameters are referred to as static or dynamic imperfections. A static impairment implies a fixed deviation regardless of vertical position of the beam on the code plate, while the magnitude of a dynamic imperfection is dependent on the beam position.

2.3.2.1 *Focusing*

The beam has a normal current density distribution with standard deviation, σ. An important parameter is the ratio W/σ where W is the length of the smallest apertures in the code plate, i.e., those corresponding to the ninth digit (Fig. 2b). When the center of the beam is positioned in the center of the aperture, the digit output current I_0 is a maximum and, conversely, I_0 is a minimum when the beam is positioned midway between two adjacent apertures. In Fig. 3, the digit output current is plotted for the ninth digit as a function of beam position with W/σ as parameter. As W/σ increases, $I_{0_{max}}$ reaches a saturated value

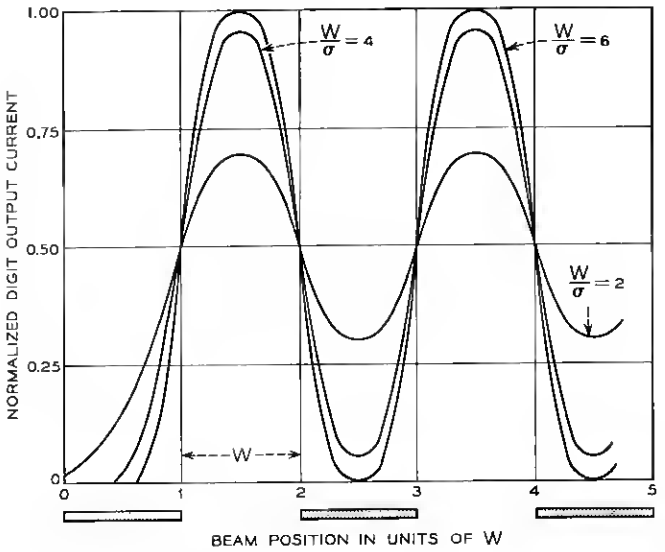

Fig. 3 — A plot of digit output current as a function of beam position. The aperture pattern is sketched below the abscissa.

and $I_{0_{min}}$ approaches zero with an increasingly steep transition between the two. This affects the final binary decision process which is performed by the output regenerator following the parallel to serial converter.

This decision circuit has a threshold level which, referred to the output level of the tube, is positioned half-way between $I_{0_{max}}$ and $I_{0_{min}}$. In practical regenerators this threshold level is the center of a finite uncertainty region bounded by $\frac{1}{2}(I_{0_{max}} - I_{0_{min}}) \pm \Delta I$. Decisions for input amplitudes which cause the digit output to fall in this region are uncertain and may result in partial output pulses, i.e., pulses having low amplitude or deteriorated rise, fall, and duration times. The likelihood of errors is further increased if the noise contributed by the digit output amplifiers to the input signal of the regenerator is considered. The implications of these effects are twofold.

First, at each transition between adjacent codes, there exists a narrow region in the input signal range over which errors are possible in those digits that undergo a change from ZERO to ONE or vice versa. A code which has the property that only one digit is changing at the transition between any two adjacent code words exhibits errors limited to less than one quantum step. For this reason, the Gray code was chosen over the straight binary code. The error is limited to less than one step and occurs

with equal probability at all 512 code transitions. The noise generated has essentially flat frequency spectrum, similar in nature to quantizing noise. The enhancement in quantizing noise has been computed for a signal with Gaussian statistics, for a regenerator with an uncertainty region of $2\Delta I/(I_{\theta_{max}} - I_{\theta_{min}}) = 0.1$, 20-dB peak signal to rms noise ratio in the digit output amplifiers, and various values of W/σ. For $W/\sigma \geqq 4$, a performance level that was readily achieved, the increment in quantizing noise is less than 0.5 dB.

A second consequence of indecision in the regenerator, and partial outputs in particular, relates to Gray code to binary code translation errors and is discussed in Section 5.6.3.

A practical coding tube usually exhibits some degree of dynamic defocusing. Consequently, at initial installation, σ is measured at various positions of the beam on the code plate for a range of external focusing bias voltages. From these data, a focusing voltage is established such that the average focus over the entire code plate is optimum. For the models of the coding tube that were used in the experimental system, average W/σ ratios in excess of 4.5 were achieved.

The beam can be focused most accurately in the center region. Defocusing effects near the edges of the beam are minimized by making the code plate narrower than the width of the beam. Also, the digits on the code plate are arranged such that those digits undergoing the most frequent transitions (digits nine, eight, etc.) are positioned in the center while digits one and two, which change less frequently, are located near the edges (Fig. 2b).

2.3.2.2 *Uniformity of Beam Current Density*

If the current density varies across the width of the beam, the digit output currents will exhibit different amplitudes. Static nonuniformity is compensated by an adjustment in each of the digit output amplifiers. This adjustment assures that the threshold for the common serial regenerator can always be set at one-half peak output current for all digits. In the tubes for the experimental system the average value of peak output current was 2.5 μA and never varied more than 10 per cent from digit to digit; usually the ninth-digit output current was lowest in peak-to-peak amplitude due to the small aperture of digit nine in the code plate. External compensation for dynamic nonuniformity in current density was not provided. The digit output current of any particular digit never varied more than ± 5 per cent as the beam was swept across the entire code plate.

2.3.2.3 *Beam Tilt*

The electron beam intersection on the code plate forms a line which should be precisely at right angles to the aperture columns. Any deviation from this angle is tilt. Static tilt can be corrected by applying an external bias voltage to the tilt correction electrodes. External dynamic tilt correction was not provided. A procedure similar to the one used for focusing is followed. A tilt correction voltage is established which minimizes the average tilt over the entire code range. After this correction is applied the average tilt usually turns out to be zero.

2.3.2.4 *Beam Bowing*

This term denotes any deviation from a straight line for the intersection of the beam with the code plate. The tubes have no provision for external correction of static or dynamic beam bowing. However, in the tilt adjustment procedure the effects of bowing can be included in the averaging process since both tilt and bowing are geometric beam imperfections and cause similar coding impairments.

2.3.3 *The Collector System*

The collector system consists of the target block with nine vertical slots in which the collector wires are located coaxially. The slots serve as an electric shield between the collector wires guarding against interdigit crosstalk.

Electrically, the digit output is represented by a current generator of 2.5 μA shunted by capacitance of 5 pF. The coupling capacitance between adjacent digits is less than 0.25 pF. The interdigit crosstalk into a particular digit from the two adjacent digits is down by more than 20 dB.

2.4 *Deflection Amplifier*

2.4.1 *General*

The design specifications for this amplifier are more severe for video coding than for mastergroup coding. For this application the principal design objectives were as follows:

(1.) The amplifier should have single-ended input and two equal-magnitude, opposite-polarity outputs, each driving a deflection plate represented by a 15-pF capacitance to ground.

(2.) Voltage excursion on each plate for full end-to-end beam deflection must be 30 V peak-to-peak.

(3.) Voltage gain from input to each output should be 18 dB and stable to within ±0.05 dB.

(4.) The transient response of the amplifier must be such that the output settles to within about 0.02 per cent (1/10 quantizing step) of its final value 60 ns after application of the sampled and held input.

(5.) Gain must be maintained to dc in order to utilize full coding range for television signals that are clamped at the horizontal sync pulse.

(6.) The input impedance of the amplifier should be 500 Ω.

For mastergroup coding (about 6-Mc/s sampling rate), the settling time could be relaxed to 100 ns and the amplifier may be ac-coupled as long as sufficient low frequency gain is provided to prevent any appreciable droop-off during the holding period.

2.4.2 *Circuit Realization*

The simplified circuit configuration of the amplifier is shown in Fig. 4. It consists of two identical forward amplifiers with common input and different feedback connections, such that the two outputs are equal in amplitude and opposite in phase.

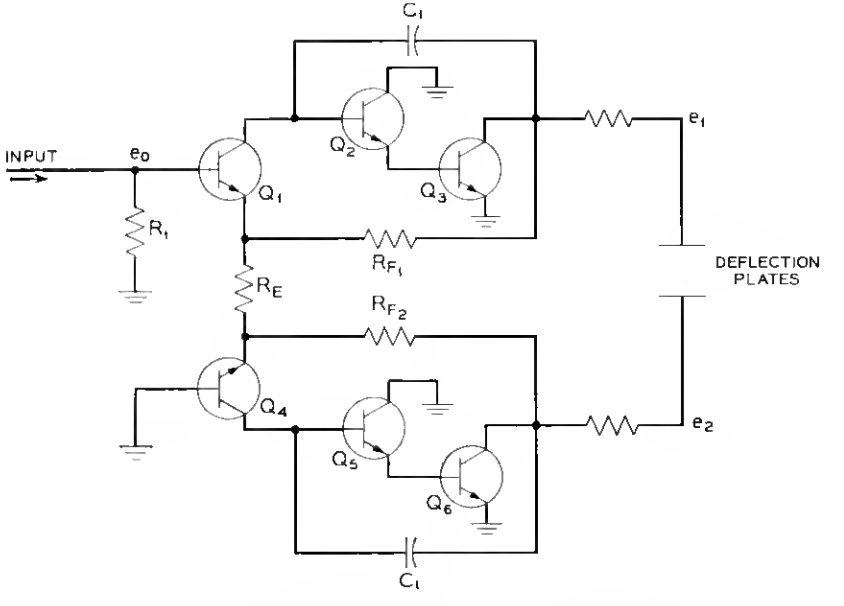

Fig. 4 — Simplified schematic of coding tube deflection amplifier.

From the feedback network the voltage gains from the input to the two outputs are established:

$$A_{V1} = \frac{e_1}{e_0} \doteq 1 + \frac{R_{F1}}{R_E}$$

$$A_{V2} = \frac{e_2}{e_0} \doteq -\frac{R_{F2}}{R_E}.$$

To make $e_2 = -e_1$,

$$R_{F2} = R_{F1} + R_E.$$

The open-loop gain-frequency characteristic is shaped with the transient response requirements of the amplifier in mind. The settling time objective is met by designing the frequency response of the open-loop current gain to have a well controlled slope of 20 dB/decade to at least an octave beyond a unity gain crossover frequency at 25 Mc/s.

For minimum gain transistors, the amplifier has an open-loop current gain of 54 dB at dc. This assures that the output settles to a steady state value with an accuracy of better than ± 0.05 dB. This loop gain is maintained up to about 50 kc/s and then falls off with the desired 20 dB/decade slope, controlled by the local feedback capacitor C_1. This is readily verified by considering the loop current gain of the lower amplifier in Fig. 4.

Breaking the feedback loop at the emitter of Q_4, the loop gain in the frequency range from 30 kc/s to about 50 Mc/s is

$$A\beta \doteq \frac{A_i Z_T}{R_{F2}}$$

where

A_i = common base current gain of Q_4
Z_T = transfer impedance from base of Q_5 to collector of Q_6.

Since Q_4 is a transistor having a gain-bandwidth product of greater than 800 Mc/s, A_i is not dependent on frequency in the range of interest and has a value near unity. The transistors Q_5 and Q_6 have gain-bandwidth products in excess of 500 Mc/s. Hence, Z_T is determined by C_1 and $A\beta$ becomes

$$A\beta(p) \doteq \frac{1}{pC_1R_{F2}}.$$

This produces the desired asymptotic performance with a unit gain frequency crossing at

$$\omega_0 = \frac{1}{C_1 R_{F2}}.$$

The 20 dB/decade slope was maintained up to about 50 Mc/s and the open loop gain then fell off with a final slope of 60 dB/decade. Since series feedback is used at the input, the input impedance of the amplifier is set primarily by resistor R_1.

The quiescent dc voltage at the output of one amplifier was fixed at -6 V. The other amplifier contains a bias control which varies the output dc voltage from -5.5 V to -6.5 V and permits external correction for any vertical misalignment of the beam. By means of this control the beam is positioned at the center code on the code plate with no input signal. Differential dc stability of the deflection amplifier outputs is important to maintain the beam at this center position. Long term differential dc stability corresponding to ± 3 quantizing steps has been achieved in the amplifier.

The physical separation between the amplifier outputs and the deflection plates is critical. Excessive lead inductance causes undesirable resonance effects. The amplifier was constructed with this in mind and installed adjacent to the tube deflection plates so that the external lead length did not exceed one inch.

2.5 *Digit Output Amplifiers*

2.5.1 *General*

The coding tube delivers a relatively low level digit output signal. The outputs are cosine-squared current pulses of 2.5-μA peak amplitude and 40-ns base width. The maximum repetition rate is about 12 Mc/s for video coding. Since it is undesirable to make binary decisions at such low levels, the output signals are amplified by linear digit output amplifiers ahead of the decision circuit.

The digit output amplifier is comprised of a low level preamplifier, which raises the signal level to 50 mV, followed by a postamplifier which delivers a 2-V peak-to-peak signal to the parallel to serial converter. Because of the low input current, it was desirable to ac-couple the stages in the preamplifier and to include a dc-restoration circuit in the postamplifier.

2.5.2 *Preamplifier*

The preamplifier is a conventional feedback amplifier consisting of three common-emitter stages and an over-all shunt-shunt feedback

network which stabilizes the input-output transresistance to 20 kΩ. The collector wires from the tube are each directly connected to the low-impedance input summing node of the corresponding amplifier. The output drives a 93-Ω coaxial cable which is terminated at the input of the postamplifier.

The amplifier has more than 32-dB loop gain at midband. The 3-dB closed-loop bandwidth of the amplifier is 25 Mc/s. This is adequate to amplify the cosine-squared pulses with only minor deterioration in wave shape.

As shown in Fig. 5, the preamplifiers are mounted directly at the head of the tube, where the collector wire output pins are located, to avoid interference and noise problems.

2.5.3 *Postamplifier*

This amplifier is similar to the preamplifier except that it is designed for higher levels and contains provisions for dc restoration. The voltage gain is feedback stabilized to 32 dB over a 3-dB bandwidth of 40 Mc/s. The input, which has an impedance of 93 Ω, is ac-coupled to the preamplifier. The amplifiers drive negative-going pulses with 2 V peak-to-peak amplitude into a 2-mA diode AND gate in the parallel to serial converter.

The base line of the output signal is restored by the dc-restoration

Fig. 5 — Digit output amplifier assembly.

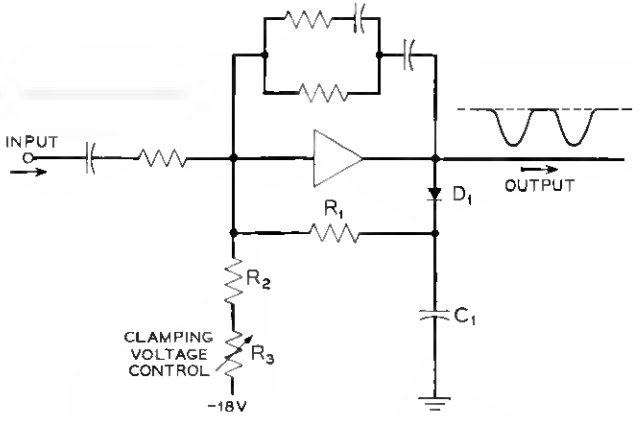

Fig. 6 — Digit output postamplifier dc-restoration circuit.

circuit to +1 V. This circuit, shown in Fig. 6, consists of diode $D1$, capacitor C_1, and resistors R_1, R_2, and R_3. The operation of this circuit is as follows:

In the absence of an input signal the dc value of the output is at the clamping voltage of +1 V. Diode D_1 is conducting and delivers positive current through R_1 into the summing node of the amplifier so as to maintain this steady-state condition. When an input signal is applied, output voltage excursions above +1 V are integrated by the capacitor C_1. This increases the dc feedback current to keep the output signal excursions below the clamping voltage.

The clamping voltage can be shifted slightly about +1 V by means of potentiometer R_3. With this control each digit output can be positioned symmetrically about a common threshold voltage which in this system is zero volts. As mentioned in a previous section, nonuniform beam current density across the width of the beam causes slightly different peak-to-peak amplitudes in the digit output pulses. The R_3 adjustment keeps the decision threshold level halfway between peak and base line on each digit.

2.6 *Associated Tube Coder Circuits*

2.6.1 *Dc Biasing*

The dc bias voltages for the tube are derived from a conventional voltage divider circuit including resistors and zener diodes. A single high-voltage supply and a filament supply are the main sources of power.

In order to avoid isolation problems in the digit output amplifiers, the digit collector wires are at ground potential and the cathode is negative. The voltage divider supplies bias voltages to the following electrodes:

(1.) cathode
(2.) control grid
(3.) focus electrodes
(4.) target block.

The electron acceleration voltage is approximately 800 V. The control grid and focus electrode voltages are externally variable. The heater power supply is floating at −800 V to prevent filament to cathode breakdown.

2.6.2 *Control Grid Driver*

The control grid is turned on towards the latter part of the holding interval by means of a 12-V peak-to-peak drive signal generated by the grid driver circuit from the sampling clock. The positive peaks of the drive signal are held flat for a period of 20 ns. The flat portion of the drive signal is desirable because at this voltage level the beam focus, which is dependent on the grid voltage, is optimized.

The input capacitance of the control grid is 16 pF. The driving circuit is a conventional two-transistor saturated amplifier which is coupled to the grid by means of a capacitor. Because the grid is at a high negative potential, the coupling capacitor has high-voltage breakdown requirements.

2.6.3 *Digital Limiter Circuit*

A PCM coder is expected to exhibit perfect limiting for an input signal which extends beyond either of the two extreme code levels. For a Gray code, one extreme level is represented by nine ZEROS, and the other by a ONE followed by eight ZEROS. In the tube coder there exists a problem with the latter. For overloads limited to several quantizing steps in magnitude, the tube coder continues to generate a ONE followed by eight ZEROS code because the aperture corresponding to digit ONE is extended somewhat beyond the extreme level. However, for excessive overload peaks the beam is deflected completely off the code plate and, in effect, generates the nine ZEROS code, which is in error by the full coding range. The resulting input-output characteristic is illustrated in Fig. 7.

This undesirable feature is eliminated by the digital limiter which is

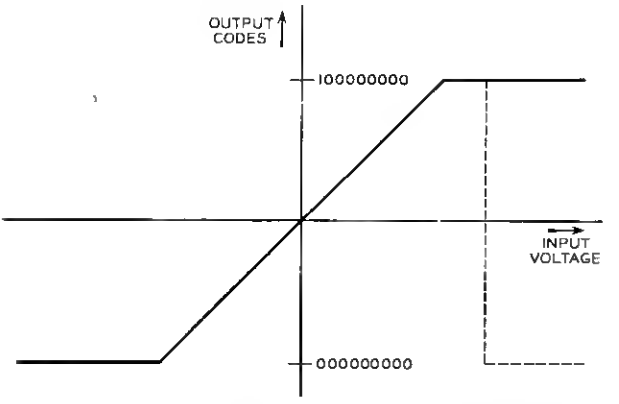

Fig. 7 — Input-output characteristic of tube coder. The dotted curve shows the transfer characteristic that results if the digital limiter is omitted.

connected as shown in Fig. 1. This circuit effectively bypasses the coding tube and forces the first digit to a ONE in the range where the problem exists.

In the Gray code the first digit is essentially the sign digit and is a ONE for the entire positive range of the signal, from level 256 to 512. The digital limiter is a wide-threshold circuit which is connected to the sample and hold output and determines whether the signal is above or below the midpoint of the positive range. If the signal is above positive half range (level 384), it forces a ONE in the output; if the signal is below, the digital limiter is effectively out of the circuit. The critical decision operation which takes place when digit one is in transition, i.e., when the signal is just changing polarity, is still performed exclusively by the coding tube.

2.7 *Performance*

The only meaningful tests of the performance of a coder are: (1.) a measurement of quantizing noise, and (2.) a measurement of errors that have large amplitudes but may occur infrequently enough so that quantizing noise is not appreciably affected. These errors may have severe subjective effects such as the appearance of occasional black or white dots on a television display.

Quantizing noise tests have to be executed in real time in conjunction with a decoder and all the associated circuitry. It is, therefore, rather difficult to establish precisely the contribution from the individual circuits to the over-all impairments. This is especially true when a

performance level very close to theoretical is reached. What circuit has to be improved when the actual performance is only a few dB below theoretical? This posed challenging questions during the experimental PCM program. However, it is most likely that the major contribution to the deviations from theoretical performance originate in the coder. Not only does this circuit perform the most difficult and critical operation, but it is also the circuit where individual tests are least likely to have meaningful results.

The tube coder was operated at 6-Mc/s and 12-Mc/s sampling rates. The theoretical and measured noise performance for 6-Mc/s mastergroup operation are shown in Fig. 8. For high input signal levels overload is controlling, and for low levels quantizing noise diminishes. Optimum loading is attained when the rms value of the mastergroup signal corresponds to about one-eighth of the peak-to-peak coding range. Under this condition, the signal-to-noise ratio is maximum and is less than 2 dB away from theoretical performance. The measurements were performed with a noise loading test set which loads the coder with Gaussian distributed bandlimited noise, and measures the total quantizing noise falling in an initially signal-free 3-kc/s channel slot. At the 12-Mc/s sampling rate, the tube coder noise performance was less than 2 dB above theoretical quantizing noise. At both sampling rates, the tube coder met the performance objective which was set at the outset of the experimental program. The performance level of the coder in regard to single errors, that are subjectively undesirable, is discussed in Section 5.6.3.

III. THE SOLID STATE CODER

3.1 *Basic Plan of Operation*

The general plan of the solid state coder was suggested by F. D. Waldhauer[6] and is an improved design based on an earlier coder described by B. D. Smith.[7] A Gray code is generated by a cascade arrangement of binary stages. Each of the binary stages must perform two functions: it must (1.) decide and report whether the applied signal is positive or negative, and (2.) deliver a residue signal to the next stage for further processing. Full-wave rectification of the input, and addition of a suitable bias so the residue ranges between equal plus and minus values, is a desirable way of presenting the residue.

Fig. 9 illustrates this process. Fig. 9(a) shows the transfer characteristic of a full-wave rectifier with gain of two. In the (b) portion of the

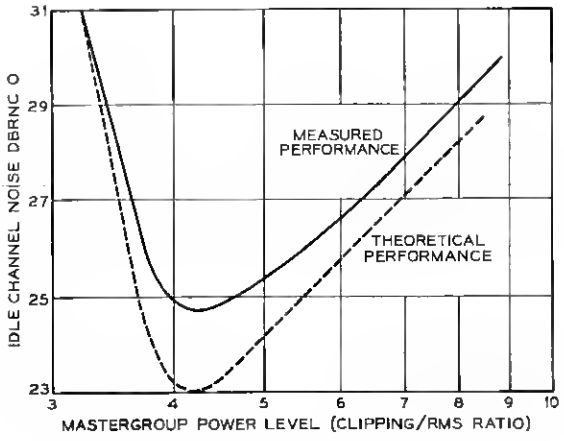

Fig. 8 — Noise performance of mastergroup codec.

figure, a one unit reference has been subtracted from the characteristic shown in (a). The digit output is a ONE when the input is positive and a ZERO when the input is negative. The amplitude of the residue ranges from -1 to $+1$. Similar stages in cascade can generate successive Gray-code digits. As in the parlor game of twenty questions, each binary decision narrows the range of uncertainty. When nine digits are known, the input can be specified within one of 512 small ranges, often called steps.

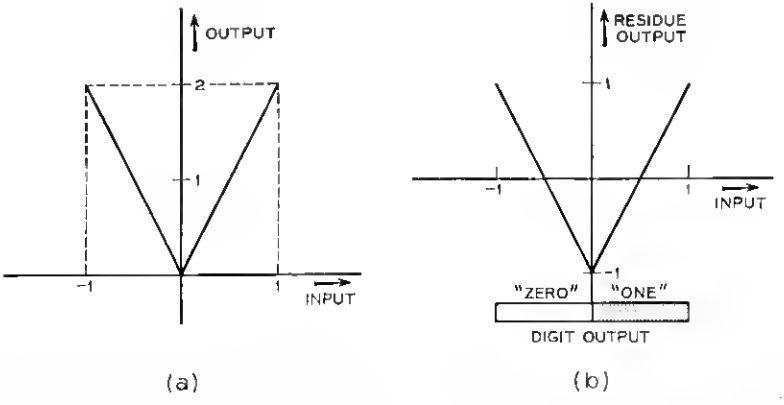

Fig. 9 — (a) Full-wave rectifier characteristic with gain of two, (b) characteristic biased with reference of one unit.

3.2 *Need for Sample and Hold*

If the input signal changes slowly with respect to the speed of the coder stages, the code corresponding to the input signal can be read out of the coder stages at any time. However, when the signal changes rapidly, the stages are unable to follow accurately and incorrect codes are generated. In order to avoid excessive speed requirements on the coder stages, the signal is sampled briefly and the sample is held constant at the input of the coder for the remainder of the interval available for coding. About one-fourth of the period (21 ns) is allowed for sampling the signal and charging a capacitor to a proportional value. The capacitor holds this value for the remaining 60 ns and applies it to the input of the coder.

3.3 *General Method of Coding*

Waldhauer[6] proposed that nearly ideal rectification can be attained by use of diodes in the feedback path of a high-gain operational amplifier. Two feedback paths with oppositely poled diodes give two half-wave rectified outputs. If the feedback is large and the diodes do not conduct in the reverse direction, the rectification characteristic is independent of diode forward drop. To obtain full-wave rectification, an inverting amplifier can be used to invert one of the two outputs. When this plan is used, the number of cascade amplifiers traversed by a signal varies with the value of the sample to be coded. This causes difficulties at high speed. Waldhauer saw that this problem was eliminated if balanced signals were fed to balanced coder stages. A typical stage is shown as Fig. 10. Two operational amplifiers are provided with rectifiers in the feedback paths. Equal and opposite input currents are applied to the two amplifiers.

Combining the outputs and adding reference currents provides balanced residues suitable for driving a following stage. A digit output circuit connected to the outputs of the operational amplifiers senses the polarity of the signal and generates a clearly defined positive or negative output with negligible chance of indecision. Figs. 10 and 11 illustrate the currents in the coder stage for positive and negative inputs.

A different circuit (Figs. 12 and 13) is used for the first stage. It is capable of taking a single ended input and producing a balanced residue suitable for driving a stage such as Figs. 10 or 11. This circuit uses partial cancellation to yield the full-wave rectifier characteristic. Figs. 12 and 13, show the circuit conditions when the maximum positive and negative inputs, $+E_M$ and $-E_M$, are applied. The delay cable is

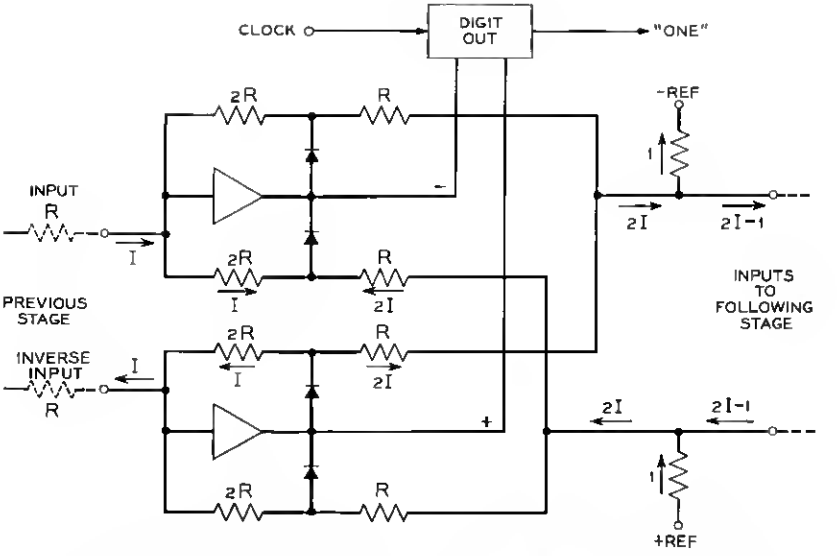

Fig. 10 — Typical solid-state coder stage, positive input.

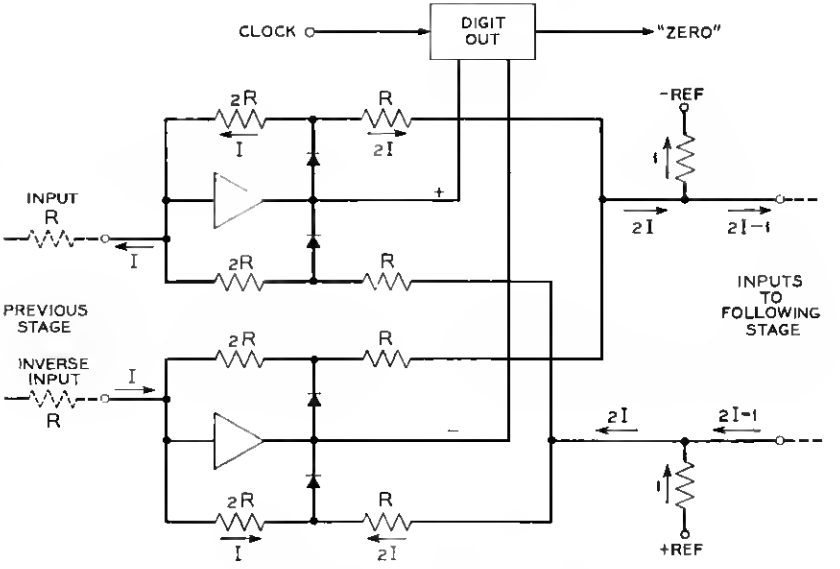

Fig. 11 — Typical solid-state coder stage, negative input.

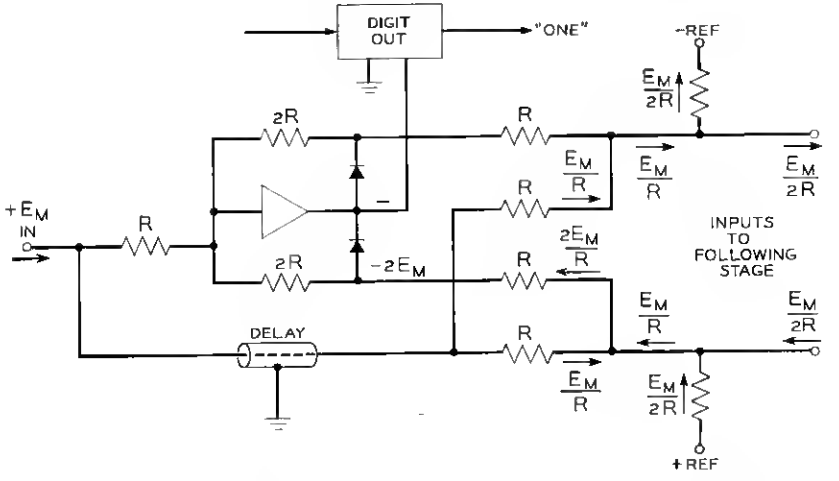

Fig. 12 — First coder stage giving balanced residue output from unbalanced, positive input.

selected empirically to match the delay of the operational amplifier. Best balance of the total output is the criterion used for delay adjustment.

When this stage is used at high speed, the operational amplifier must have a transient response such as to settle very nearly to the final steady-

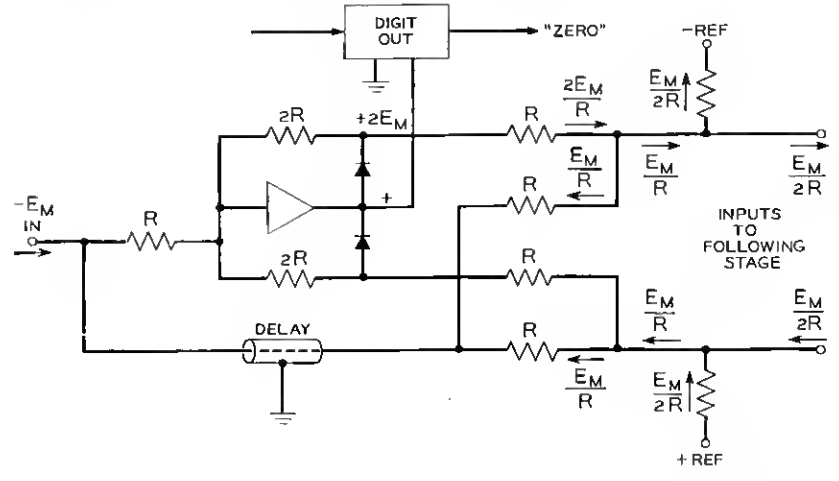

Fig. 13 — First coder stage giving balanced residue output from unbalanced, negative input.

state value in the allowed 60-ns interval. This requires a loop gain which slopes off uniformly at 20 dB/decade and has a unity-gain crossover frequency as high as can be attained. A unity-gain crossing at 80 to 90 Mc/s has been realized. This gives a settling time constant of 2 ns. The gain may roll off more rapidly above the unity-gain crossover frequency without seriously deteriorating the transient response. The amplifiers used in this coder have a minus three slope (60 dB/decade) which sets in about half a decade above the unity-gain crossover frequency. Deviations from the desired unit slope in the three decades below the unity-gain crossover frequency are more serious. They can produce relatively slow transients that are not of negligible amplitude.

An additional high-speed problem is introduced by the transition from one feedback path to the other when the output changes sign. The forward drop required to cause the decision diodes to conduct requires the amplifier output voltage to change by twice this value before current can be diverted from one diode to the other. If the input changes from a large value to a small value of opposite polarity, the amplifier output moves exponentially until one diode cuts off. Next, the output moves linearly at the same rate until the opposite diode conducts. Then the exponential approach to final value is resumed. Time required to cross the midregion may be longer than a sampling interval if the diode drop is large in relation to the signal swing. This difficulty can be reduced only at the expense of some reduction of static accuracy. The means for improvement is to bias the diodes in the forward direction so that, with no input to the coder stage, some current flows in each of the decision diodes. The feedback path does not fully open and the change of output voltage required to cross over is much reduced. The rectification characteristic (Fig. 9a) is rounded at the point of the "VEE" and does not reach zero. This makes the decision problem more difficult for the digit output circuit, and inputs near the decision point deliver a less accurate residue to the succeeding stages.

3.4 *Computer Analysis of Coder*

The result of forward bias on coder performance was studied by simulation on the digital computer assuming amplifiers with an ideal unit slope which becomes a three slope starting half a decade above the unity gain point. The diodes were assumed to follow the ideal exponential law. These studies show that forward bias improves transient response at the expense of static accuracy and makes a very large reduction in rms error of coding. All stages were assumed to have the same bias. Because of coder stage gain, this means that maximum error

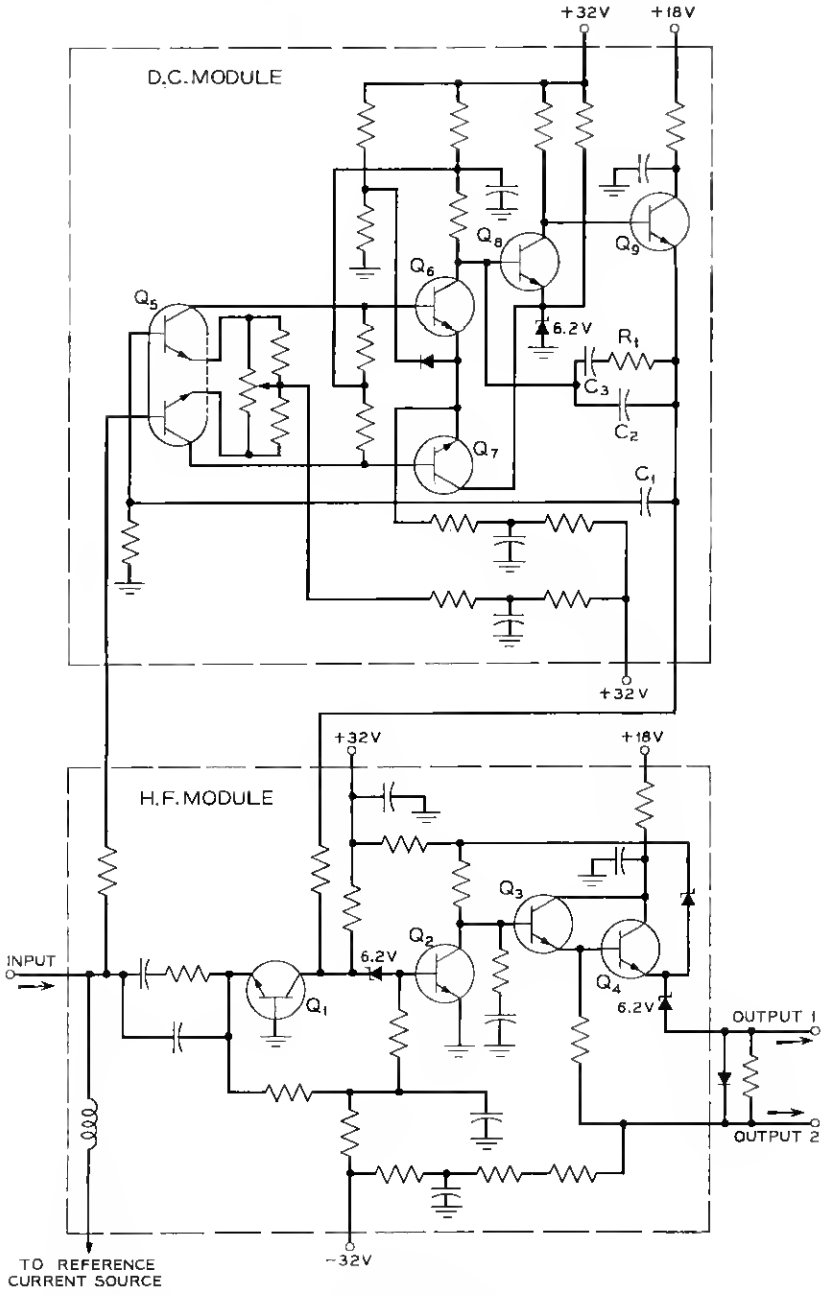

Fig. 14 — The composite operational amplifier.

occurs in the two decision points adjacent to the center transition. Bias in the first stage does not inherently introduce error in the center decision or most significant digit, though it does make the decision problem more difficult and so increases the random error and drift at this decision point. The errors caused by bias, expressed as a fraction of a step, tend to be halved in each successive stage. There are, of course, twice as many opportunities for error in each successive stage if all input amplitudes are equally likely. Thus, for a signal with flat probability distribution, the error power contribution of all succeeding stages would equal that of the first. With a normal distribution, as provided by a mastergroup of single sideband telephone channels, the first stage error would dominate.

For the normal distribution of input signals, the optimum bias is such as to move the decision points adjacent to the center by about one-half step. Increase of bias to eliminate the two center codes, or even four center codes, does not cause serious deterioration of system performance if judged by rms error.

3.5 *Circuit Design of the Operational Amplifiers*

Circuit design features of the operational amplifiers were discussed by F. D. Waldhauer.[10] If the desired accuracy of transient settling is to be attained, the open-loop gain must maintain substantially unit slope over a range of about six decades below the frequency of unity transmission. Some pole-zero pair cancellations may be tolerated in the lower three decades but the upper three decades must be extremely clean. The amplifier must also be nearly free of drift and noise. The design chosen is such that a current of 13 μA applied at the input represents a change of one code step. Drift resulting from temperature and aging over a reasonable maintenance interval must be less than one-tenth of this value.

Stable, low-drift, dc transistors do not have good wideband performance. Thus, the problems are solved separately and suitable circuits are joined as sbown on Fig. 14. The high-frequency transmission path is througb a four-stage amplifier comprising a common-base stage, a common-emitter stage, and a compound common-collector stage. This ampfilier has the desired single phase reversal at low frequency and from about 100 kc/s to over 100 Mc/s the amplification varies inversely with frequency. The collector-to-base capacitance of Q_2 is dominant in controlling the gain slope. Bootstrapping the power feed resistors to the output preserves the very high input impedance of the compound common-collector output stage.

In broadband amplifiers, excess phase caused by transit time is very important. Each transistor tends to add about 0.1 ns. In the cordwood modules used in the first coder, wiring length added about three inches which translates to 0.3 ns. Later models used multiple-chip integrated packages containing the four high-speed transistors and two breakdown diodes providing a 6.2-V drop. The shorter path length and better controlled stray capacitance resulted in substantially smoother high frequency transmission characteristics.

To continue the gain slope below 100 kc/s and to provide low dc drift, a dc amplifier takes over transmission from the common-base stage. The first stage is a differential pair of matched transistors contained in a single encapsulation. Mounting the two transistor chips in one package minimizes differences of V_{BE} with variation of temperature. This stage is followed by a second balanced stage using large common-emitter resistance to maintain constant total current. One collector of the second stage drives the base of a common-emitter third stage. The output stage is common-collector.

Variations of V_{BE} in transistors Q_6 and Q_7 are not very important, provided they are less than 100 mV. Therefore, mounting the transistors in a common encapsulation is not necessary. Drift in the balance of current input required by the second stage is very important, because any such unbalanced input must be provided by the first stage. For this reason the operating current is reduced to about 6 μA for each transistor. Reduction of the total current also reduces the possible unbalance. The transistor was chosen to maintain large current gain at very low current. The first stage operates from a relatively low source impedance so current gain is less important and V_{BE} is very important. Current to each half of Q_5 is about 50 μA. With this design, the initial balance takes care of dissymetry in transistors and other components and subsequent drift is small in terms of a peak input of 3.3 mA to a coder stage.

The feedback capacitor C_1 gives the dc amplifier a unit slope for about four decades from 100 c/s to over 1 Mc/s. The gain value is such that the transmission through the dc amplifier, and that of the common-base stage of the high-frequency amplifier merge at about 100 kc/s and produce a zero to match the pole of the high-frequency amplifier.

If the gain of the dc amplifier continued to fall off smoothly with a slope of 20 dB/decade, no further compensation would be needed in the mid-frequency region. The transistors used in the first stages are of limited bandwidth so the gain slope must increase to 60 dB/decade at about 2 Mc/s. Even though the high-frequency path dominates in this frequency region, the change of slope of the low-frequency path

produces a small doublet in the over-all transmission characteristic and can cause noticeable degradation of transient behavior. Local feedback by capacitors C_2 and C_3, and resistor R_1 reduces this effect, but it may still be significant. Further study is needed.

3.6 *Digit Output Circuits*

When the coder transients have settled, it is necessary to read out the states of the individual stages and generate a corresponding code word. The code is read out on nine parallel lines approximately simultaneously. These outputs are brought into time coincidence by suitable lengths of cable and directed to the parallel to serial converter.

It is important that the code pulses delivered shall be definitely binary in nature. Indecisive or partial pulses can result in serious errors in Gray to binary translation and decoding. The process of forcing a decision is commonly called regeneration. It is usually done by the use of trigger action involving negative resistance in some form. For best results, the negative resistance circuit should be very fast compared to the time allotted for decisions. For this reason, it has been placed in the digit output circuits, where the code is handled in parallel and more time is available for decision.

The circuit now in use is shown is Fig. 15. The differential input stage can be driven balanced or single sided. Suitably biased limiter diodes in the collector circuit prevent saturation of the transistors on the one excursion and limit the positive swing on the other. The input impedance presented to the coder stage is a few hundred ohms for small signals near the decision point and much higher for inputs of 50 mV or more regardless of polarity. It does not load the coder stage.

The second stage (Q_3 and Q_4) serves the dual purposes of amplifier and gate. The emitters are held at a static potential of about +6.4 V by a bias regulator circuit. This is comparable to the maximum base voltage permitted by the catcher diodes in the first stage so current cannot flow to Q_3 or Q_4 in the absence of additional emitter drive. The 12-Mc/s clock signal is supplied to Q_7, which runs as a limiter, and the small pulse-forming capacitor of 10 pF drives the emitters of Q_3 and Q_4 in a negative direction for a period of a few nanoseconds. A pulse of current flows to one or both of transistors Q_3 and Q_4, depending on the input to the first stage.

The tunnel diode has a peak current of 5 mA and a valley current of about 0.5 mA. Resistors connected to the +32-V and −12-V power supplies together with a center tapped pair of resistors across the tunnel

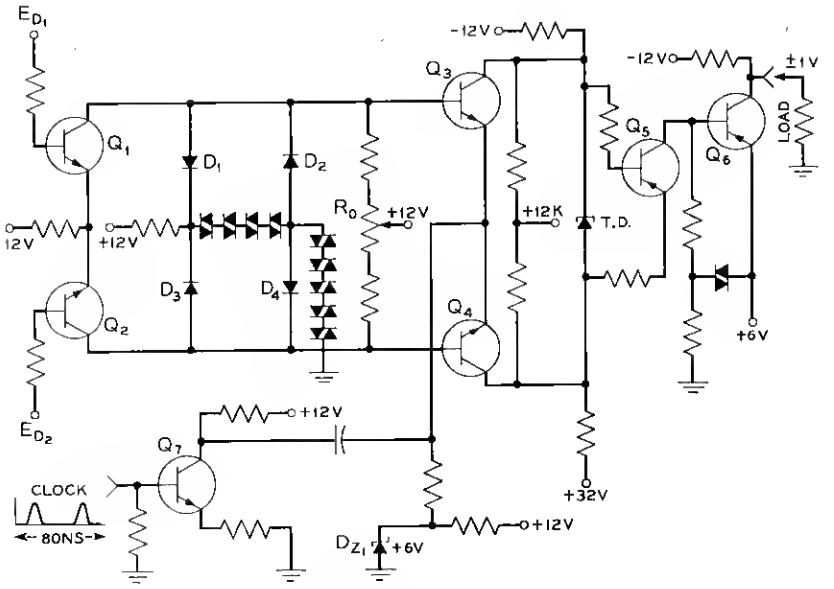

Fig. 15 — Solid-state coder digit output circuit.

diode provide bias equivalent to an 870 Ω, 2.56 V source which is balanced with respect to +12 V. The negative slope resistance of the tunnel diode is much less than 870 Ω so the circuit is strongly bistable.

When the clock pulse turns on Q_3 alone, the tunnel diode is forced into its high-current state. If Q_4 alone is turned on, the tunnel diode goes to the low-current state. If the currents of Q_3 and Q_4 are equal, or differ by too small an amount, the state of the tunnel diode remains unchanged after the clock pulse passes. These marginal inputs do produce a disturbance; but it dies out rapidly. The timing is arranged so that the output is gated into the serializing line in a 5-ns interval immediately preceding application of the next following clock pulse to Q_3 and Q_4. Thus, the tunnel diode circuit has about 70 ns in which to form a decision. The probability of residual indecision is very small. However, to meet system requirements it is necessary to use an additional serial regenerator (as in the case of the tube coder) to further resolve decision uncertainties (see Section 5.6.3).

3.7 *Experimental Results*

The nine-digit coder was built using precision resistors with ±0.02 per cent tolerance in the feedback, feed forward, and reference bias

positions. The dc amplifiers were trimmed by means of the potentiometer between emitters of first stage so that the voltage at the summing node of every stage was less than 50 μV. Static alignment was then attained by trimming the reference resistors of all stages. This was done by applying specified dc inputs corresponding to the successive decision levels and observing the state of the coder stage being adjusted. The work progresses from the first-digit stage to the ninth-digit stage. Initial adjustment was made to a precision of 1/20 step or better. Static accuracy is maintained over a period of months with errors no more than ± 0.1 step in most cases and a maximum of ± 0.15 step. This source of error would not degrade the noise performance by more than 1 dB from theoretical nine-digit performance.

When the coder is operating at a sampling rate of 12 Mc/s into a decoder whose imperfections are known to be small, the measured peak-to-peak signal to rms quantizing noise is 57 dB which is 7 dB more noise than would be expected from a perfect nine digit system. When the sampling rate was cut to 6 Mc/s, corresponding to operation on a mastergroup, the performance was 28 dBrnc0, which is within 5 dB of theoretical nine-digit quantizing noise. The rms error was reduced to about three-quarters of its former value because twice as much time was allowed for the transients to settle. It is believed that imperfect matching of the dc amplifier and the high-frequency amplifier is an important contributor to the noise impairments. A second coder with improved amplifiers is in process of construction.

IV. Associated Coder Circuits

4.1 *Sample and Hold*

4.1.1 *General Description of Sample and Hold Circuit*

Fig. 16 shows in block form the method used to carry out the sampling and holding process. The input signal passes through an amplifier whose output impedance is only a few ohms. The amplifier output is switched to the holding capacitor C by driving balanced currents through a diode bridge. When the bridge current is cut off, the charge on the capacitor is held. The capacitor provides an input to an amplifier whose input impedance is about 1 MΩ. With 100-pF capacitance the time constant is 100 μs; so the droop of the held voltage is about one part in a thousand in an 80-ns interval. In the following discussion, the more difficult 12-Mc/s sampling operation for the solid-state coder will be emphasized.

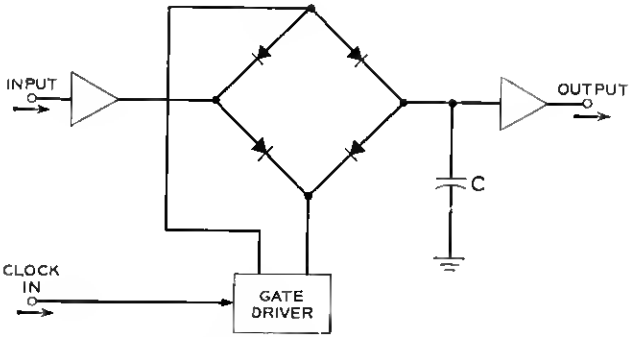

Fig. 16 — Sample and hold.

4.1.2 *Analysis and Requirements*

If the gate driver could supply a constant current to the diode bridge for the sampling period (about 21 ns) and then instantly switch the diodes off and into a state of back bias greater than the signal voltage, perfect operation would depend only on diodes with negligible storage time and very high back resistance. Hot-carrier diodes satisfy these requirements well enough. If the driver changes the bridge voltage slowly, the diodes cut off at different times unless the signal is zero. This results in some change in the charge stored on the holding capacitor during the turn off time. This, in turn, aggravates the transient settling problem of the coder and also produces some nonlinearity in the sampling process. To keep the nonlinear distortion well below quantizing noise, the driver needs to switch the gate off in less than 1 ns. This requirement is documented in the paper by Gray and Kitsopoulos.[11]

4.1.3 *Preamplifier and Postamplifier*

The preamplifier is of straightforward design using shunt feedback to provide constant gain, linearity, and low output impedance. Its load impedance is switched from open circuit to 100-pF capacitance. The preamplifier must be stable under both load conditions and have good transient performance.

The postamplifier is more critical in design. High input impedance is obtained with a transistor amplifier by using series feedback at the input and designing for unity voltage gain. The loop gain varies inversely with frequency (unit slope) up to about 50 Mc/s. This results in good transient response and in an equivalent input impedance of 1 MΩ in parallel with a 10-pF capacitance.

4.1.4 *Gate Driver Pulse Forming Network*

The pulse forming portion of the driver is shown on Fig. 17. Balanced direct currents I_0 are applied through resistors from the plus and minus 32-V supplies. The magnitude of I_0 is 15 mA. This current will flow through the bridge or be diverted through diodes $D5$ and $D6$ depending on the voltage generated by the driver.

Sinusoidal current at the desired sampling frequency of 6 Mc/s or 12 Mc/s is introduced through blocking capacitors C_1 and C_2 and flows through inductors L_1 and L_2 to the pulse-forming diode network. The peak value is 0.6 A. Direct bias current is introduced through L_3 and L_4 with a value of about 0.4 A so that the total current tends to forward bias $D12$ for 25 per cent of the time and to forward bias $D11$ for 75 per cent of the time. These diodes are of the type which exhibit charge storage and snap recovery properties. While $D12$ is conducting in its forward direction, with a peak current of about 200 mA, stored carriers accumulate in the semiconductor. As the current reduces to zero and reverses direction, these carriers tend to maintain conductivity and hold the voltage drop almost constant at the value that existed when it was conducting in the forward direction. This situation persists for about 4 ns with reverse current sweeping out the stored charges. Then, within a period of 0.2 or 0.3 ns, conductivity "snaps" off and reverse current no longer flows. By this time the reverse current has built up to a value of about 160 mA and is still growing since the inductors L_1 and L_2 insure

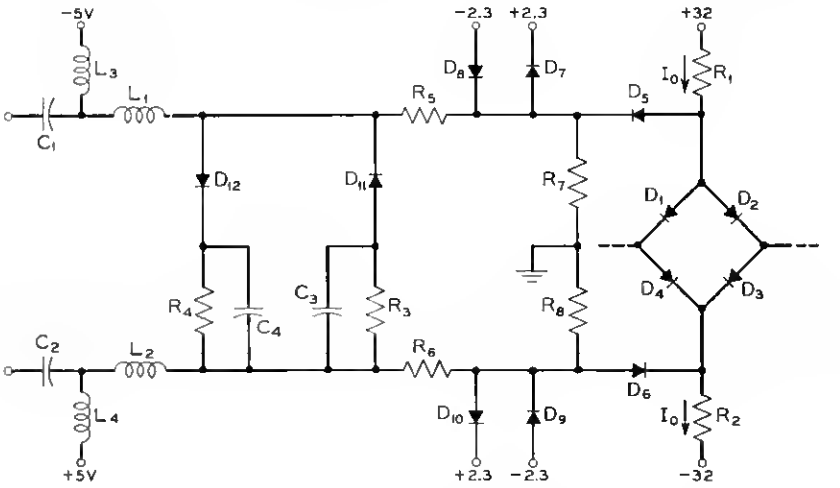

Fig. 17 — Sample and hold gate driver pulse forming network.

tbat the fundamental component dominates and the harmonics are small. When $D12$ snaps off, the large current is immediately available to charge the stray capacitance (about 4.5 pF) and to overcome the bias voltage and diode drop establishing current in $D11$. $D11$ is also a snap diode but capable of working with larger average current. It operates in the same manner as diode $D12$ except that it serves to steepen the step that takes place wben current switches from diode $D11$ to diode $D12$. Average currents flowing througb R_3 and R_4, bypassed by capacitors C_3 and C_4, provide back bias on tbe diodes of about 6 V. Thus, the voltage from line to line must swing about 14 V to transfer conduction from diode $D12$ to $D11$ or vice versa. The more important transition from $D12$ to $D11$ (the onset of the holding portion of the cycle) takes almost 1 ns; the other is a little slower. Diodes $D7$–10, supported by resistors R_5 and R_6, cut the output sligbtly so the voltage presented across R_7 and R_8 to ground swings ± 3 V. Tbese diodes clean up tbe top portions of the waveform and serve to establisb a low impedance at high frequencies from each side of tbe bridge to ground while the bridge diodes are in the cut off state. This aids in establishing a large loss from the source to the holding capacitor during the holding interval so that the held voltage is maintained constant.

4.1.5 *Power Amplifier for Gate Driver*

The power amplifier tbat provides the sine-wave drive is shown in Fig. 18. Design need not be covered in detail. The tuned circuits are not very high Q; so variations of phase shift have not proven troublesome. Shielding is essential in the interest of preventing unwanted oscillations and to keep the large circulating currents from getting into the coder. Tbere is quite a bit of beat generated but it has caused no serious problem.

The common-base first stage is used only to provide a good impedance to the clock source. The push-pull common-emitter second stage provides power gain to drive the final amplifier. The push-pull output stage operates in the common-base mode. This may not be immediately apparent because the collectors are grounded. It was necessary to solidly ground the cans (and thereby the collectors) for heat transfer. Using isolation windings on the interstage transformer permits the base and emitter to swing. The stage is operated class B for convenience and efficiency.

4.1.6 *Mechanical Layout*

As is the case in all higb-speed circuits, the mechanical layout of the sample and hold circuit is an important part of the total electrical de-

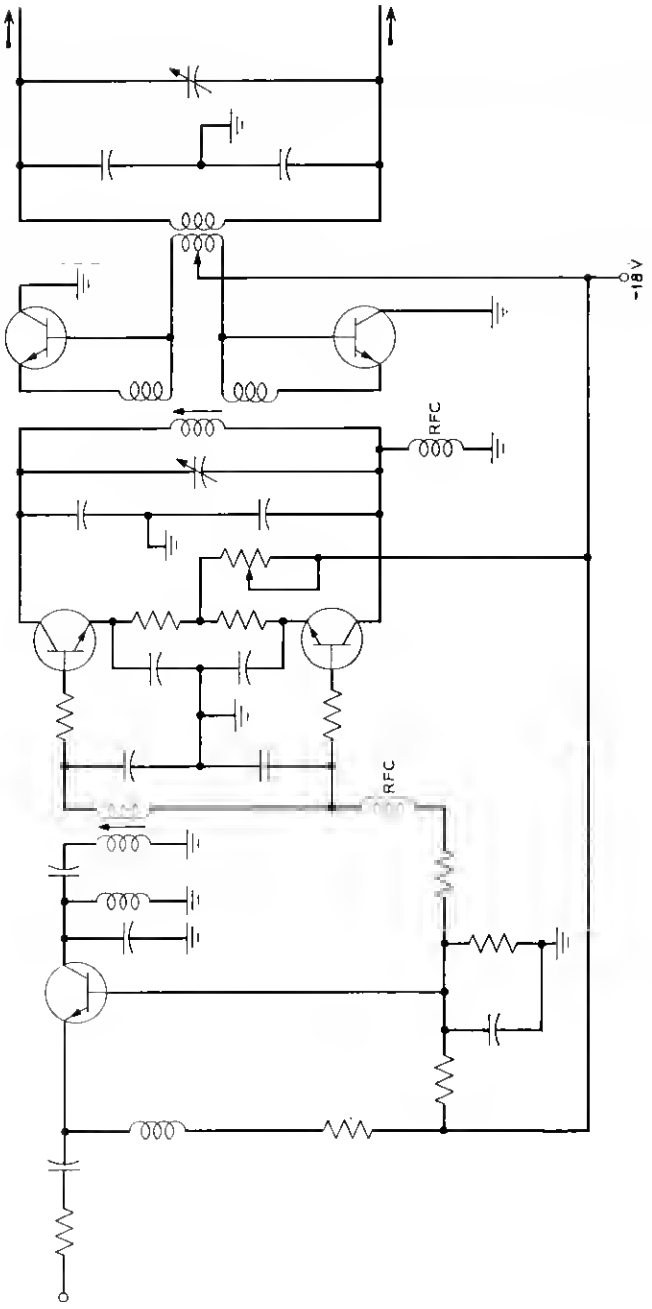

Fig. 18 — Sample and hold sine wave power amplifier.

sign. The photograph (Fig. 19) shows one view of this circuit. Complete symmetry of the bridge is important. The preamplifier and postamplifier are mounted close to the bridge as are the final pulse forming parts of the driver. The entire circuit is enclosed in a solid shield.

4.1.7 *Performance of Sample and Hold*

When tested separately with the resampler only, the sample and hold circuit gives a noise performance at least 6 dB better than an ideal nine-digit system. It does not appear to limit system performance at present. It is somewhat difficult to adjust for good performance but once adjusted has performed well over long periods of time. Simpler driving circuits are under investigation.

4.2 *Parallel to Serial Converter*

The digit output circuits of both the tube and the solid-state coder present the PCM code words as plus or minus voltages on nine separate leads. All outputs are in phase and occur periodically at the sampling rate. The parallel to serial converter combines these signals into a serial pulse train. This process is carried out by means of a tapped delay line.

Fig. 20 illustrates this operation for the case of the 12-Mc/s converter. Each digital output is sampled by a 4-ns clock pulse and gated onto the respective tap of the delay line. To avoid reflections, the line is terminated at both ends in its characteristic impedance. The total end-to-

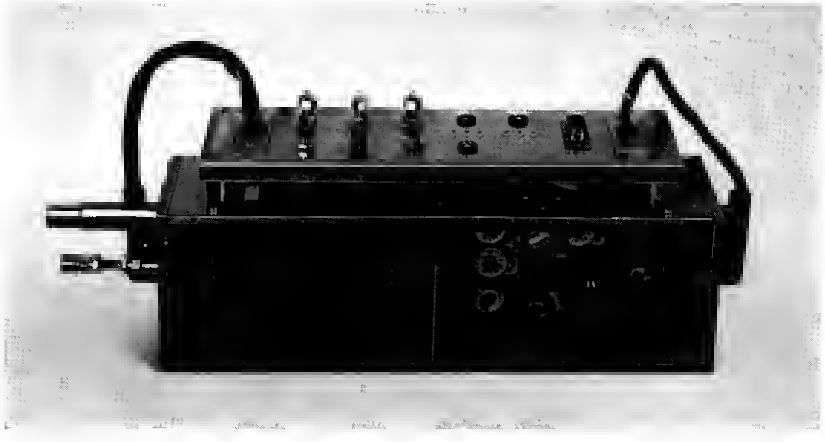

Fig. 19 — Sample and hold.

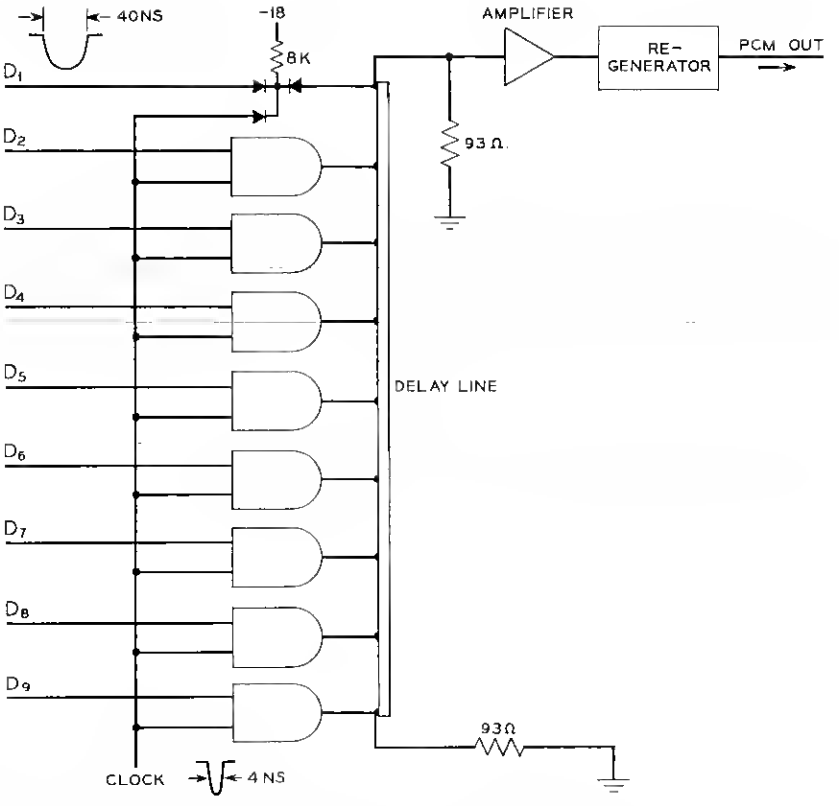

Fig. 20 — Parallel to serial converter.

end delay of the line is 72 ns, divided into eigbt sections of equal lengtb. At the upper termination of the line the signal appears in serial form; digit one first, digit nine last. A linear dc amplifier of 200-Mc/s bandwidth raises tbe output signal to a level of 2 V peak-to-peak.

A partially shielded microstrip delay line of somewhat unconventional construction was used. Fig. 21 is a photograph of this line. A dielectric material is sandwiched between a ground plane and a conductor plane. However, the conductor plane contains an additional ground area that is interleaved with the conductors. This construction reduces coupling between adjacent sections of the conductor, permits a closer spacing between conductors, and hence larger amounts of delay are realizable in a given area. The line is photoetched on a 1/16-in. thick copper clad Tellite board, whose dimensions are 12 in. by 16.5 in.

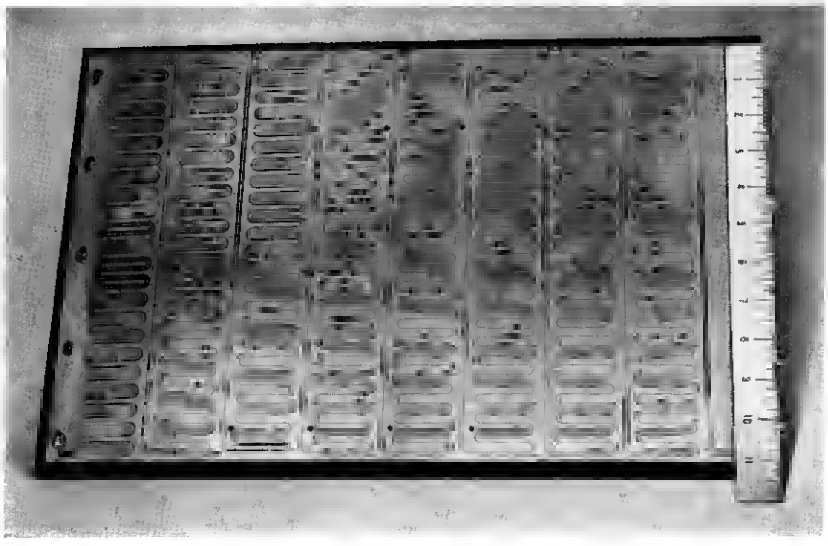

Fig. 21 — Partially shielded microstrip delay line.

The characteristic impedance of the line is 93 Ω. The response to a 4-ns pulse is excellent. The total end-to-end attenuation of 2 dB is somewhat higher than the attenuation of a coaxial cable of the same electrical length. However, this line has a definite advantage over a coaxial line because the conductor is exposed and, therefore, the taps can be connected without any difficulties and without the introduction of appreciable discontinuities in the line.

A source of reflections on the line is the load that the gates present to their respective tapping points. When a gate is conducting, the load is the 8-kΩ gate resistor; when a gate is not conducting the load is the capacitance of the output diode, which is less than 0.5 pF. The two load conditions represent impedances that are high compared to the 93-Ω line impedance. The total reflections on the line are 20 dB below the signal.

In the 6-Mc/s converter, which requires a delay of 144 ns, a coaxial cable line was used. A microstrip delay line with that much delay would have unwieldy dimensions and excessive end-to-end transmission loss.

4.3 *Output Regenerator*

The function of the regenerator is twofold. It makes the final binary decision on the output digits, i.e., it resolves the remaining partial, or

undecided digits that may still be present at this point. Second, it retimes and reshapes the serial output pulses. It must be a relatively fast circuit, since it executes these functions on 4.5-ns pulses. As will be discussed in a later section, the threshold uncertainty region must be extremely small. Achievement of such speed and accuracy dictates the use of 2.5-Gc/s transistors in conjunction with tunnel diodes.

Fig. 22 is a partial circuit schematic which shows the threshold and retiming circuit. Fig. 23 illustrates the composite current-voltage characteristic of the tunnel diode $D1$ and transistor Q_1. It includes the actual operating points of the circuit for various input conditions. These points are readily derived from the circuit parameters.

Transistor Q_1 can be turned on only when both the signal and the clock are negative to their respective thresholds (operating point A). Even if the signal subsequently rises positive with respect to its above threshold (as may be the case for a partial undecided digit pulse), the transistor remains in the "on" condition (point B) until the clock signal crosses its threshold. Q_1 then turns off (point C). Under the remaining two input conditions (D and E), Q_1 never turns on. The timing of the regenerator is shown in Fig. 24.

This circuit ensures that the output pulsewidth is determined exclusively by the clock, regardless of the width of the input signal. The use of the tunnel diode as a threshold element makes this circuit extremely fast and results in a very narrow threshold region.

The threshold performance of this circuit cannot be measured directly.

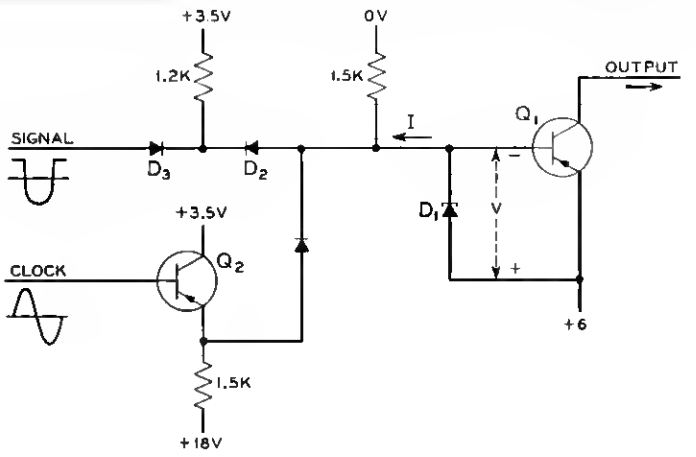

Fig. 22 — Regenerator threshold and retiming circuit.

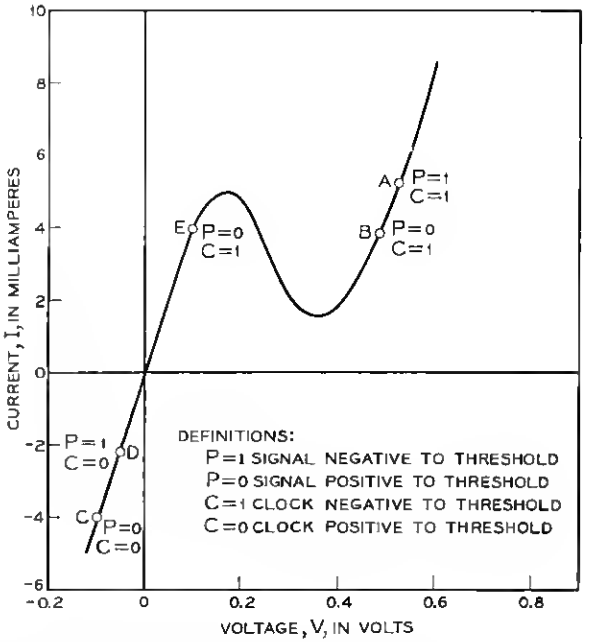

Fig. 23 — V-I characteristics of threshold circuit shown in Fig. 22. Operating points for various input conditions are shown.

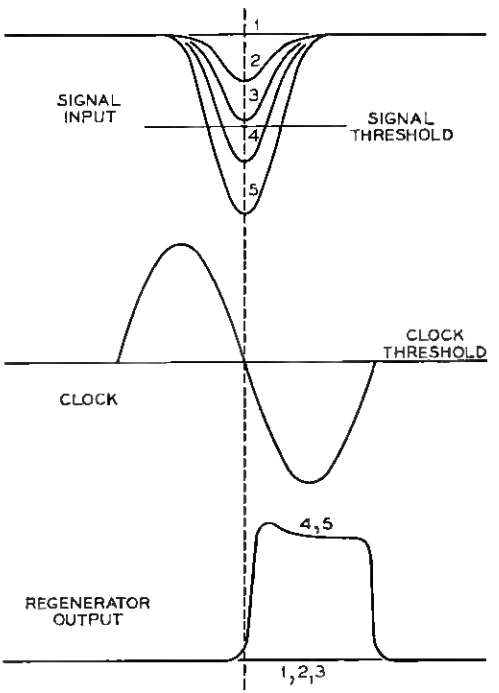

Fig. 24 — Timing of regenerator. The input signal wave shape illustrates the effect of partial pulses.

All attempts to do this have lead to the erroneous conelusion that tbis regenerator is ideal; which it is not. However, the error performance of tbe entire system will give a elue to the actual performance. This will be discussed further in Section 5.6.3.

4.4 *Clock Circuits*

Tbe video coder as well as the mastergroup eoders have individual sine-wave elocks. The clock signal is generated by means of a crystal-controlled Colpitts oscillator. The desired stability is achieved by mounting the crystal in a temperature-controlled oven.

The sine-wave clock is distributed, via 93-Ω coaxial cable, to the various points in the system from conventional emitter-follower distribution amplifiers. Proper timing is obtained by suitable choice of line-length.

A times-nine multiplier eircuit (Fig. 1) generates the elock signal used for timing the output regenerator. Tbe video eoder has an additional eircuit that divides the sampling clock by a factor of eighteen for purposes of forced-bit framing (Seetion 5.5.1).

4.5 *Bandlimiting and Reconstruction Filters*

The mastergroup signal is inherently sharply bandlimited and therefore the filter design is straightforward and presents no problems. On the other hand, the television signal falls off rather slowly with frequeney and the filter design for this applieation is more diffieult. It is controlled by the transmission objectives for television. Both the bandlimiting filter and the reconstruetion filter for television were designed by balancing foldover distortion against transient behavior and making minor refinements to satisfy the over-all transmission objeetives. The bandlimiting filter is implemented by a seventh-order Butterworth filter with delay equalization, and tbe reconstruetion filter is a fifth-order inverse Tchebycheff filter also with delay equalization.

V. DECODING TERMINAL CIRCUITS

5.1 *General*

The deeoder executes the digital to analog conversion process at the receiving terminal. Fig. 25 shows a block diagram of the receiving video terminal. The Gray-code serial PCM pulse and its timing signal are received from the demultiplex terminal. By means of a countdown circuit the frequency of the reeeived high-speed (approximately 110

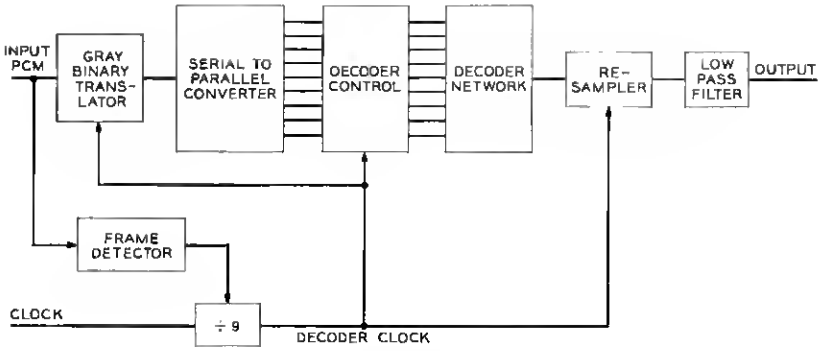

Fig. 25 — Decoding terminal.

Mc/s) clock signal is divided by a factor of nine. This process yields the 12-Mc/s clock signal which is used to time the various decoding circuits. The terminal framing detector controls the countdown circuit and thereby ensures that the clock signal has the correct phase relationship with respect to the information pulse train.

The information digits, after being processed by the Gray to binary translator and the serial to parallel converter, are read into the decoder control circuitry.

The actual digital-to-analog conversion process takes place in the decoding network. The output of this network is then fed to the resampler and the low-pass filter.

The mastergroup decoder is identical with the video decoder except all operations are executed at one-half the speed and the framing method is different.

5.2 *Decoder*

The decoder consists of: (1.) the decoder control circuits, (2.) the weighting network, and (3.) the resampler. The decoder control circuits are nine storage flip-flops into which the parallel binary PCM word is read. The weighting network (Fig. 26) is a resistive ladder network with eight sections, each of which has a transmission ratio of two. Under control of its corresponding storage flip-flop, each network node is supplied with a current of $+I$ or $-I$, depending on wether the stored digit is a ONE or a ZERO. The voltage generated at the output of the network, as a result of the individual node currents, has a magnitude which corresponds to the PCM word. The network output is then resampled.

Maintenanee of constant loss ratio in the ladder network depends on keeping a eonstant resistance at eaeb node independent of the value of the digit. The gate shown on Fig. 26 presents a resistanee R when the flip-flop is in either the ONE or the ZERO state. Use of $+E$ or $-E$, rather than E and ground, gives network outputs witb equal plus aud minus swings. In the design of the weighting network the shunting effeet of resistanee R must be considered.

E. F. Kovanie[12] has diseussed the design and operation of the video deeoder in detail. The reader is referred to his paper for further information on this subject. Only minor modifieations have been made in the deeoder control circuitry; but, the resampler was redesigned entirely and is discussed in Seetion 5.3.

The mastergroup decoder utilizes an integrated tantalum-nitride thin-film network. The design requirements and the fabrication of this network are described elsewhere.[13] The diodes that switch the network eurrents are eneapsulated in groups of four in a single paekage. These are appliqued to the thin-film network. A photograph of the mastergroup deeoder, ineluding the network, is shown in Fig. 38.

The integrated thin-film approaeh to the realization of the network has several advantages over the diserete resistor approaeh. The geometry of the integrated network permits a reduction in parasitic elements, espeeially induetanee; thereby redueing ringing in the analog output. The entire paekage is eonsiderably smaller in size and use of the common substrate yields better temperature tracking of the resistors.

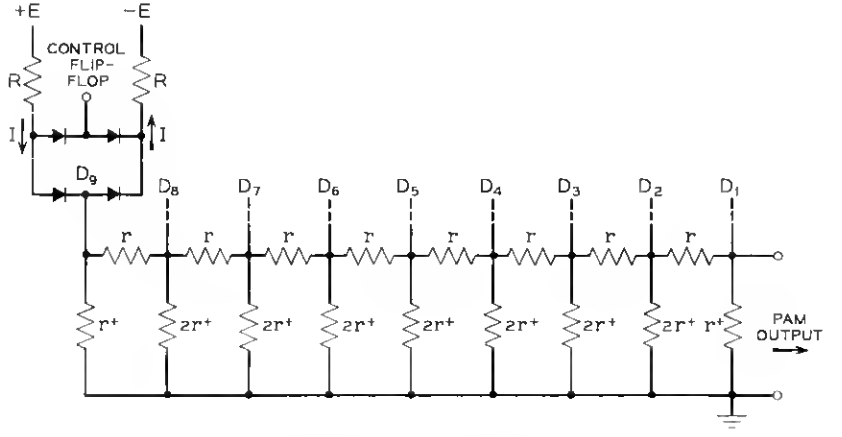

Fig. 26 — Decoder weighting network.

5.3 *Resampler*

5.3.1 *Function*

The resampler substantially eliminates all switching transients that are present in the decoder PAM output signal. These transients occur in the form of spikes when the PAM signal changes from one quantizing level to another. In a practical decoder, these transition spikes are unavoidable because the nine network currents, that are under the control of the digits, cannot be switched simultaneously in an infinitessimal time. These spikes are not linearly correlated with the signal. Their energy is dependent on which and how many digits are being switched. For example, a transition from code 011111111 to 100000000, which represents a change of only one quantizing level, at the center of the coding range in the binary code causes the largest spike because all digit currents are switched. If these spikes were not removed, the signal impairment would be substantial.

5.3.2 *Requirements*

The resampler is basically a transmission gate which conducts only during that portion of the PAM sample that is free of transients. For video decoding the gate periodically conducts for a 28-ns interval.

To avoid further degradation in over-all system performance as a result of the resampling process, the total signal distortion due to the resampler is held to a value which is better than 10 dB below quantizing noise. Transmission impairments in the resampler are caused by: (1.) distortion in the input and output amplifiers, (2.) nonlinearities in the gate, and (3.) signal compression which is a result of finite switching time. This latter condition is quite important because the output signal, after it has passed through the low-pass filter, is proportional to the area under the resampled PAM pulses. For infinitely fast rise and fall times this area is linearly proportional to the pulse amplitude; but for finite gate switching times this is not the case. For a PAM pulse width of 28 ns, gate switching time must be less than 4 ns.

5.3.3 *Circuit Description*

A schematic of the resampler is shown in Fig. 27. It consists of an input amplifier, a balanced diode gate, an output amplifier, and a gate driver. The gate is a balanced diode bridge, similar to the sample and hold gate, which works into the summing node of the output amplifier. Since this amplifier is a shunt-feedback amplifier with more than 40 dB of

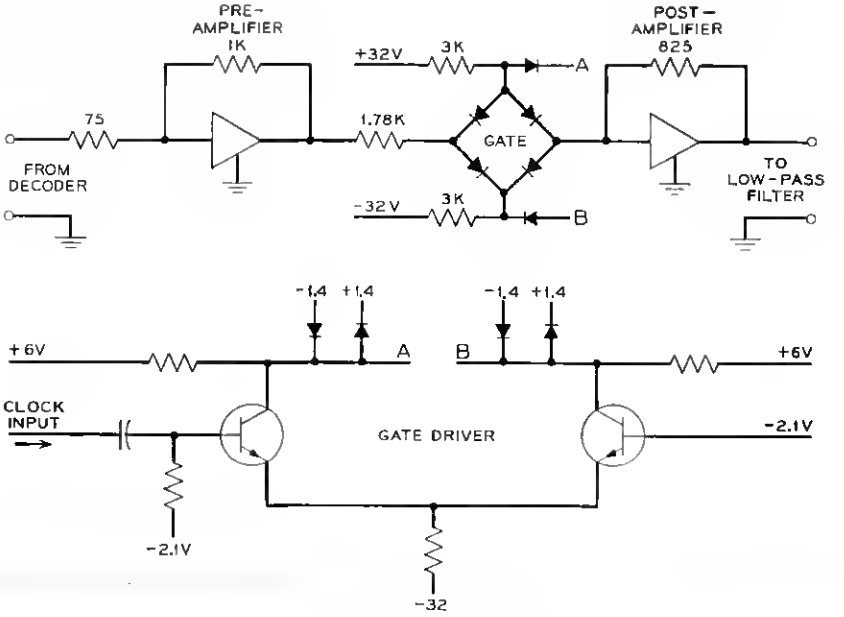

Fig. 27 — Resampler circuit.

loop gain, the impedance looking into the summing node is very low. On the other side, the gate is driven from the input amplifier through a 1.78-kΩ resistor. This impedance is high relative to the summing node impedance that the gate sees at its output. As a result, the gate is switching signal current into a virtual short circuit, rather than switching a signal voltage into a finite impedance. This has several advantages.

This mode of operation makes the gate relatively insensitive to the effects of an error voltage which may exist between the input and output of the gate as a result of mismatched diodes. Because of the relatively high impedance in the gate transmission path, the error voltage has negligible effect on the gated signal current. This considerably reduces the magnitude of a pedestal which an error voltage would introduce into the gated signal if the gate were to operate in the voltage mode. By the same argument, the impedance of the bridge, which is nonlinear because of the diodes, introduces negligible degradation to the transmission performance.

The current mode of operation has further advantages in regard to the switching performance. The gate is switched in a similar fashion to the sample and hold gate. However, since the resampler, in contrast

to the sample and hold gate, works into a virtual short circuit, the voltage excursions at the input and output nodes of the bridge are extremely small and centered around the quiescent dc voltage which is adjusted to a value of zero volts and has less than 10-mV drift. Consequently, if the gate is driven by control pulses that are reasonably symmetrical in shape with respect to each other, all diodes switch very nearly simultaneously (Fig. 28). The rise time of the control waveforms may be relaxed provided symmetry and summing-node voltage drift is under control.

The circuit that generates the control pulses is a current routing circuit (Fig. 27). This circuit generates pulses which have opposite phase and excellent symmetry. The pulses are clamped to ± 1.7 V and have a rise time of 10 ns. Ideal current-mode operation of the gate is achieved if (1.) the dc voltage at the postamplifier summing node is zero volts, (2.) the two gate control pulses cross zero at the same instant, and (3.) the postamplifier summing node is a short circuit so that the voltage excursions of the gated signal are zero. In the system, deviations from these ideal conditions were held to within ± 100 mV. In this case, the theoretical switching time of the gate is 0.6 ns. Because of the finite switching times of the diodes, the actual gate switches somewhat more slowly. The gate diodes are gallium arsenide switching diodes with less than 1-pF junction capacitance and negligible storage time.

The noise performance of the resampler was measured with a noise-loading test set. The noise level is more than 10 dB below the quantizing noise of a theoretical nine-digit coder.

5.4 *Serial to Parallel Converter*

This circuit is similar to the parallel to serial converter. Identical delay lines are used. The serial pulse train is fed into one end of the line and the parallel outputs are taken from the tapping points by means of single-stage emitter followers.

Strictly speaking, the outputs do not contain the digits in parallel

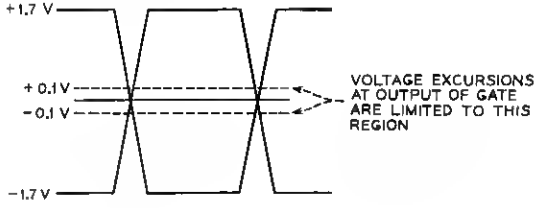

Fig. 28 — Resampler gate driver wave shapes.

form, but instead, each output lead contains the serial pulse train delayed one time slot from the preceeding output lead. At the decoder control circuit all nine outputs are sampled simultaneously by a single clock pulse. In this way the proper digits are gated to their respective decoder circuits.

5.5 *Framing Detector*

5.5.1 *Television Framing*

The television codec is framed by removing the ninth digit of every ninth word at the coder and substituting ONES and ZEROS alternately. This introduces a small degradation in over-all system noise performance.[1] At the decoder the framing detector identifies the framing pulses and ensures that the decoder timing clock has the proper phase relationship with respect to the received digits. The framing detector is patterned after the framing circuit used in the T1 carrier system.[14]

A simplified functional block diagram is shown in Fig. 29. The approximately 110-Mc/s clock received from the demultiplex terminal is divided down by a factor of 81 to produce a clock at the frame rate. The frame clock gates a pulse out of the high-speed line. This pulse is compared with a reference flip-flop which generates the framing pattern. If the system is out of frame, violations occur and are sent to the store. After an average of about three violations have occurred, the threshold

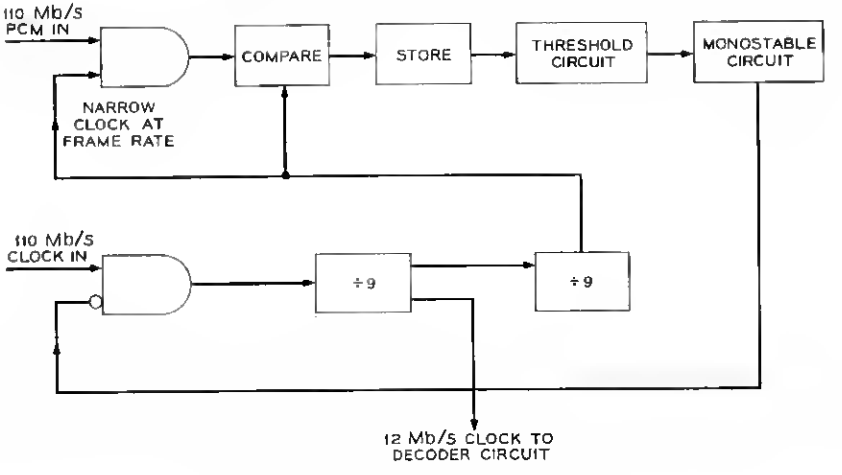

Fig. 29 — Video codec frame detector.

circuit recognizes an out of frame condition and sends an error pulse which in turn inhibits the high-speed clock and shifts the counter by one time slot. This process is repeated until the system is in frame.

The worst case exists when the decoder timing has slipped by only one time slot. The decoder framing detector has to advance the decoder timing a slot at a time through 80 time slots until it is in frame again. It checks for a framing digit every $9 \times 81 = 729$ ns. If it is assumed that any information digit has a 50 per cent probability of being in the same state as the framing digit, it takes on the average about 1.5 μs to advance one time slot. Since 80 time slots have to be traversed before the decoder is in frame again, the average reframe time is $1.5 \times 80 = 120$ μs. Fig. 30 shows experimental data on the distribution of reframe time in the worst case.

5.5.2 *Mastergroup Framing*[15]

The mastergroup codec is framed by observing the statistics of the digits in the received Gray-code pulse train. If the coder is loaded with

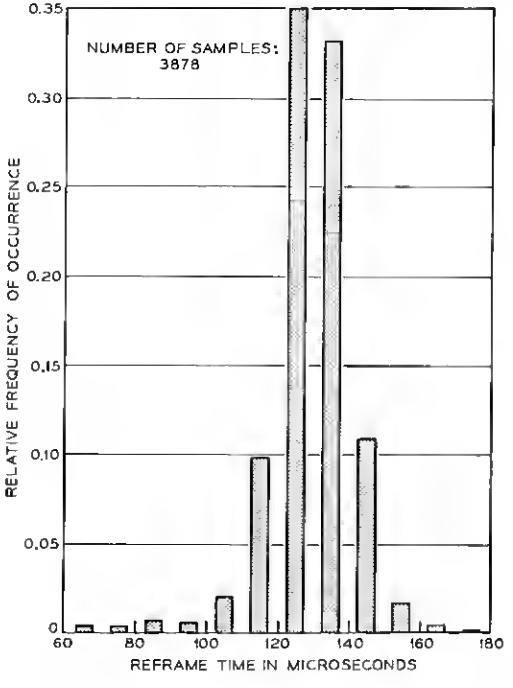

Fig. 30 — Distribution of video codec reframe time in worst case.

a mastergroup signal, which has Gaussian amplitude distribution and an rms value of one-eighth the peak-to-peak coding range, digit two has a 95 per cent probability of being a ONE while the probability of a ONE in any other digit position is nearly 50 per cent (Fig. 31).

The block diagram of the framing detector is shown in Fig. 32. The approximately 55-Mc/s clock is divided by a factor of nine. This process yields the basic decoder clock at the sampling rate. This clock periodically extracts a digit from the signal pulse train. If the extracted digit is a ZERO, the clock pulse also charges a leaky integrator. If the extracted digits have the value ZERO frequently enough, the integrator reaches the threshold value and sends out a shifting command to the countdown circuit. When the receiver is finally in frame, the integrator will remain below the threshold because of the infrequent occurrence of zeros in digit two.

Measured data of the reframing time statistic in the worst case (when timing slips only one digit) is given in Fig. 33.

5.6 *Gray to Binary Translator*[16]

5.6.1 *General*

The coders generate the Gray code because, as previously mentioned, the probability of gross error in coding is thereby made negligibly small. Since the binary code is more simply decoded, the code must be trans-

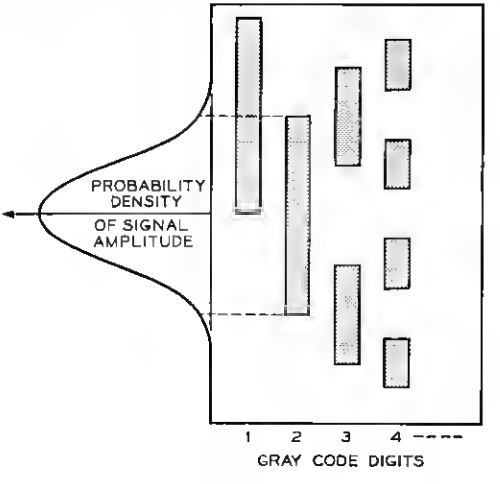

Fig. 31 — Gray-code digit assignments.

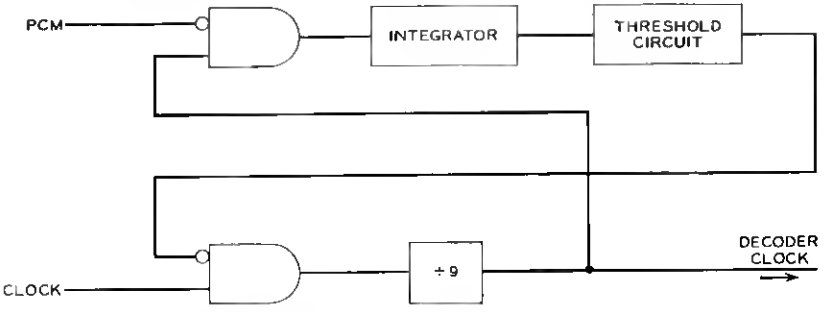

Fig. 32 — Mastergroup codec framing detector.

lated. As will be discussed in Section 5.6.3, the translator produces gross errors when partial pulses are presented at the input. In order to take advantage of the circuits in the multiplex and demultiplex terminal and the repeatered line to further resolve undecided pulses, the translation is performed at the receiving end. The amount of circuitry required is considerably less when the translation is performed on the serial pulse

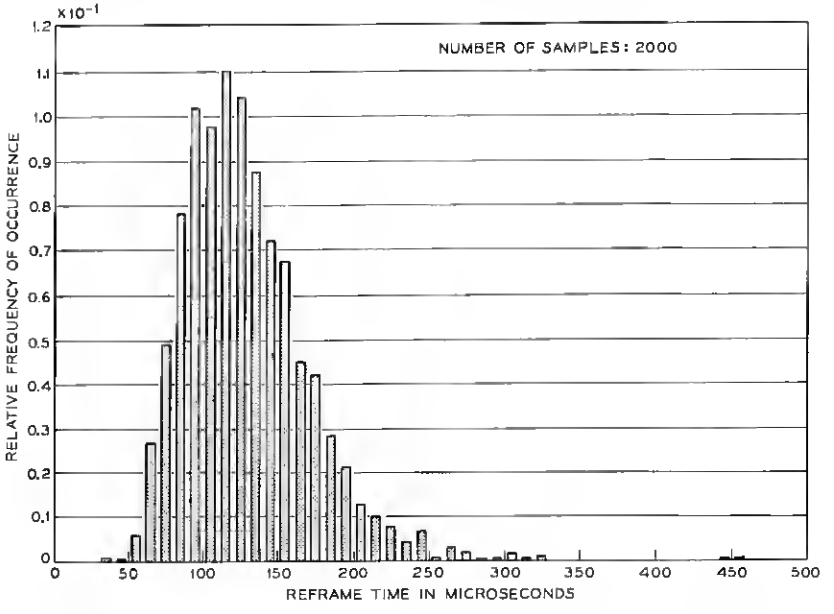

Fig. 33 — Distribution of mastergroup codec reframe time in worst case.

stream rather than in parallel, although the speed requirements are quite stringent.

5.6.2 *Circuit Realization*

Let b_k and g_k represent tbe $k$tb digits in tbe binary and the Gray-pulse streams respeetively. Let n be the number of digits in a serial word. The translation logie is

$$b_1 = g_1$$
$$b_k = b_{k-1} \cdot \overline{g_k} + \overline{b_{k-1}} \cdot g_k$$

for

$$2 \leqq k \leqq n.$$

The second equation states that binary digits other than the first repeat the preceding binary digit if the Gray-code digit is ZERO and are inverse to the preceding binary digit if the Gray-code digit is ONE. This function is represented by the output of a flip-flop, or binary counter, which can be forced to agree with the first digit and is then free to be triggered by subsequent ONES in the Gray-code word.

The desired logic function is realized as shown in the block diagram of Fig. 34. The actual circuit schematic is shown in Fig. 35. The circuit operates with a speed of 110 Mc/s. It employs germanium mesa transistors which have a gain-bandwidth product of 2.5 Gc/s. The duration and position of the clock pulses is critical and must be controlled to a small fraction of a time slot.

5.6.3 *Effect of Partial Pulse on the Translation Process*

A cause of translation errors is the presence of an unresolved partial pulse at the input of the translator. A partial pulse has deteriorated wave shape and represents neither a binary ONE nor a ZERO. The magnitude of the error depends on which digit is unresolved. The largest error occurs in the case of a partial first digit and the error magnitude decreases for suhsequent unresolved digits. To illustrate the mechanism by whieh these translation errors are generated, the ease of a partial first digit is considered.

Suppose the sample at the input to tbe coder has an amplitude level which is preeisely midway in tbe coding range. The coder is expected to process this sample into the code word 010000000 (quantizing level 255) or 110000000 (quantizing level 256). However, because the coder as well as subsequent threshold circuits are not ideal, the state of the

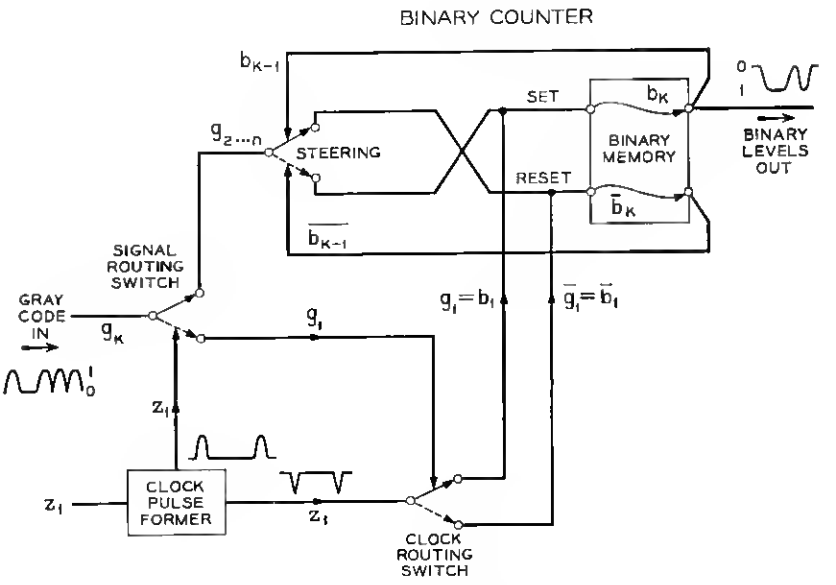

Fig. 34 — Serial Gray to binary translation.

first digit may not be completely resolved and a code which may be called $\frac{1}{2}10000000$ and has a partial pulse in the first digit position appears at the translator input.

The first digit controls the clock routing switch which directs the clock pulse Z_1 to the set or reset inputs of the binary memory (Fig. 34). Since the first digit has partial energy, this operation may not be executed properly. The binary cell may momentarily change state, but, because of insufficient trigger energy, will return to its previous condition. Therefore, the partial pulse has propagated to the output of the translator. The output of the translator is simultaneously directed to two different destinations: (1.) the decoder control circuit, and (2.) the steering switch. An undecided translator output may result in one of the following situations:

(1.) Both the decoder and the steering switch interpret the translator output as a ONE (or a ZERO). In this case no error is made and the word is correctly decoded as quantizing level 256 (or 255).

(2.) The decoder interprets the output as a ONE while the steering switch interprets a ZERO (or vice versa). In this case the resulting binary code is effectively 111111111, which corresponds to quantizing level 512 (or the binary code is 000000000, which corresponds to quantizing level ZERO).

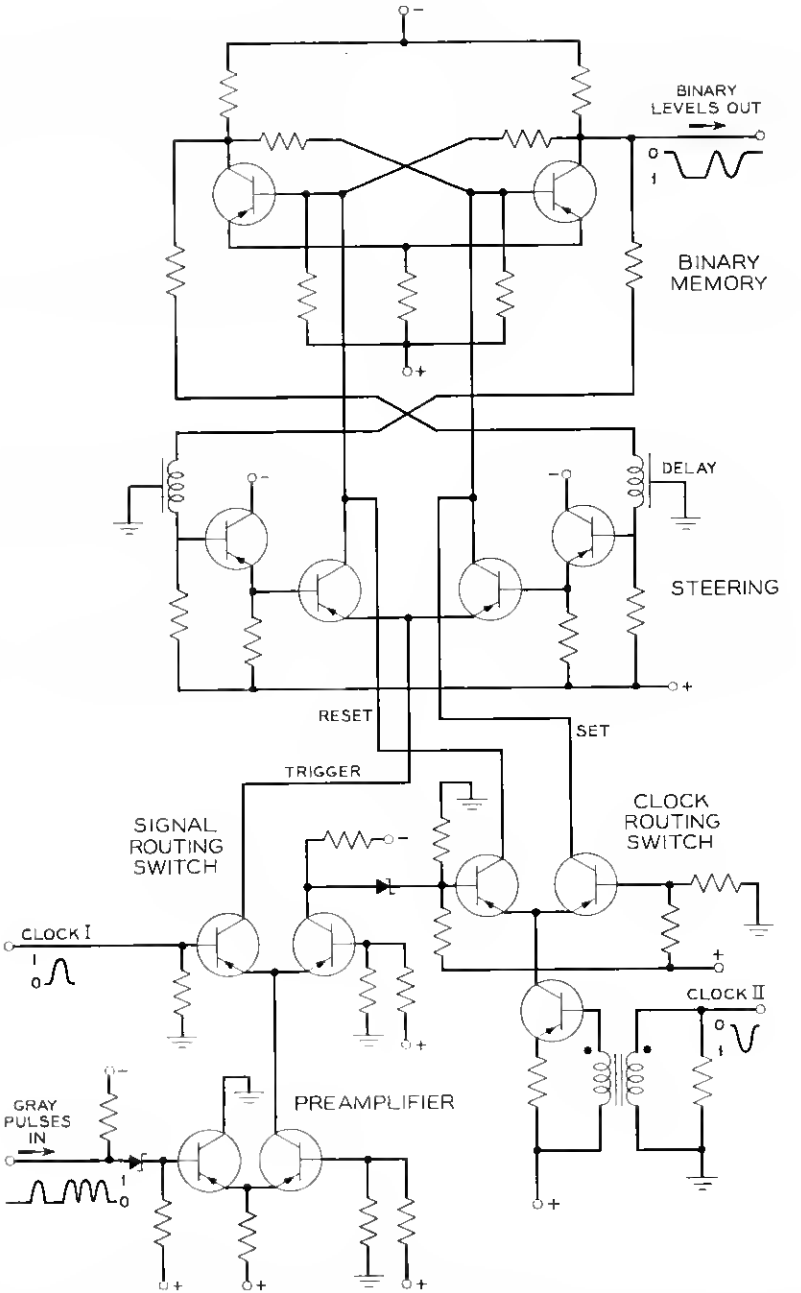

Fig. 35 — Gray to binary translator.

Because of the inconsistency in the decisions reached by the two circuits, an error with a magnitude of one-half the coding range is made. A similar error mechanism exists for partial pulses in the second-digit time slot. These errors have a magnitude of one-quarter the amplitude of the coding range.

These errors occur relatively infrequently and therefore do not affect the noise appreciably. However, when they occur, they are, because of their large amplitude, clearly visible in the form of occasional white or black dots in a decoded television display.

In order to see how sharp the effective threshold of the entire system must be for a tolerable error rate, the width of the threshold uncertainty region over which first digit errors occur is computed. For a standard television signal, the video signal excites about 366 codes; the remaining 146 codes are coding the sync pulses. Of the 720-million samples coded every minute only 600 million contain video information; the remainder are used for the sync pulses. If it is assumed that the video information has uniform amplitude distribution, the width of the uncertainty region over which first-digit errors occur must be held to within six parts in 10^7 for an error rate of one error per minute.

This level of performance has been achieved in the experimental system.

VI. EQUIPMENT DESIGN

The codec equipment is mounted on four standard 19-in. relay racks. The major equipment features are depicted in the photographs (Figs. 36 and 37). Except for the coding tube and the video decoder, the circuits are mounted on small plug-in cards and in 16.5-in. by 12-in. sliding drawers. The latter appears to be the most promising approach for a design for manufacture. Fig. 38 is a photograph of the drawer that houses the decoder. The basic design encompasses a large printed circuit motherboard onto which small circuit packages and other components are mounted. By this approach the system can be divided into major functional blocks which have relatively few interconnections. Within each major block the more numerous interconnections between the subsystems are done with little difficulty on the motherboard. The high-frequency signals are brought in from the outside via RG 180/U coaxial cable and are transmitted to their destination by means of microstrip lines on the motherboard. The extensive use of microstrip lines for interconnection of subsystems reduces the amount of bulky coaxial cables and associated connectors.

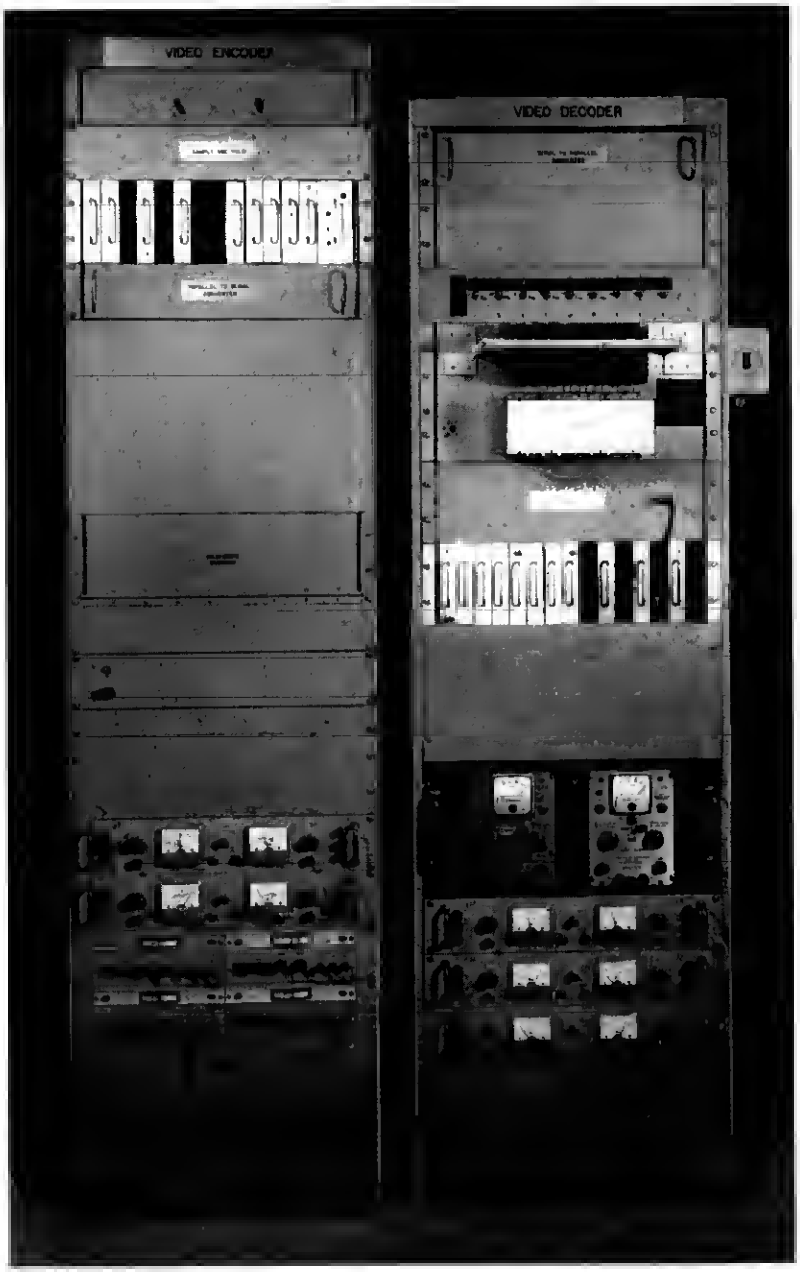

Fig. 36 — Video codec.

Fig. 37 — Mastergroup codec.

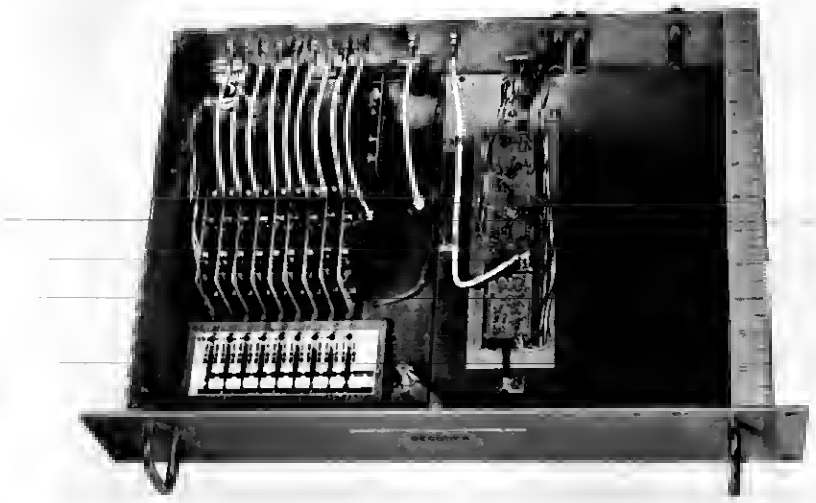

Fig. 38 — Decoder.

VII. CONCLUSION

Codecs for the PCM coding and decoding of a 600-voice channel, frequency division multiplexed, mastergroup and of a standard color or black and white television signal have been built and operated successfully. The practicability of commercial designs of such codecs and their associated circuitry has been demonstrated.

For mastergroup coding (6-Mc/s sampling rate), the theoretical quantizing-noise level under optimum load conditions is 23 dBrnc0. The measured noise of the over-all systems was 25 dBrnc0 with the tube coder and 28 dBrnc0 with the solid-state coder.

For television coding (12-Mc/s sampling rate) the theoretical peak-to-peak signal to rms noise ratio is 64 dB (including 1-dB framing impairment). The measured peak-to-peak signal to rms noise is 62 dB for the tube coder and 57 dB for the solid-state coder. Improvement in the performance of the solid-state coder should be possible with additional work.

VIII. ACKNOWLEDGMENTS

This work represents the efforts of several people and was carried out in the PCM Terminal Department under the direction of J. S. Mayo. The success of this project would not have been possible without

the active support of several device and components departments. We are particularly indebted to M. H. Crowell and his associates who developed the nine-digit coding tube and to the Thin Film Components Department under the direction of D. A. McLean for the development of the decoder thin-film network.

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